

Compal Confidential

Model Name : P5WE0

File Name : LA-6901P

BOM P/N:43

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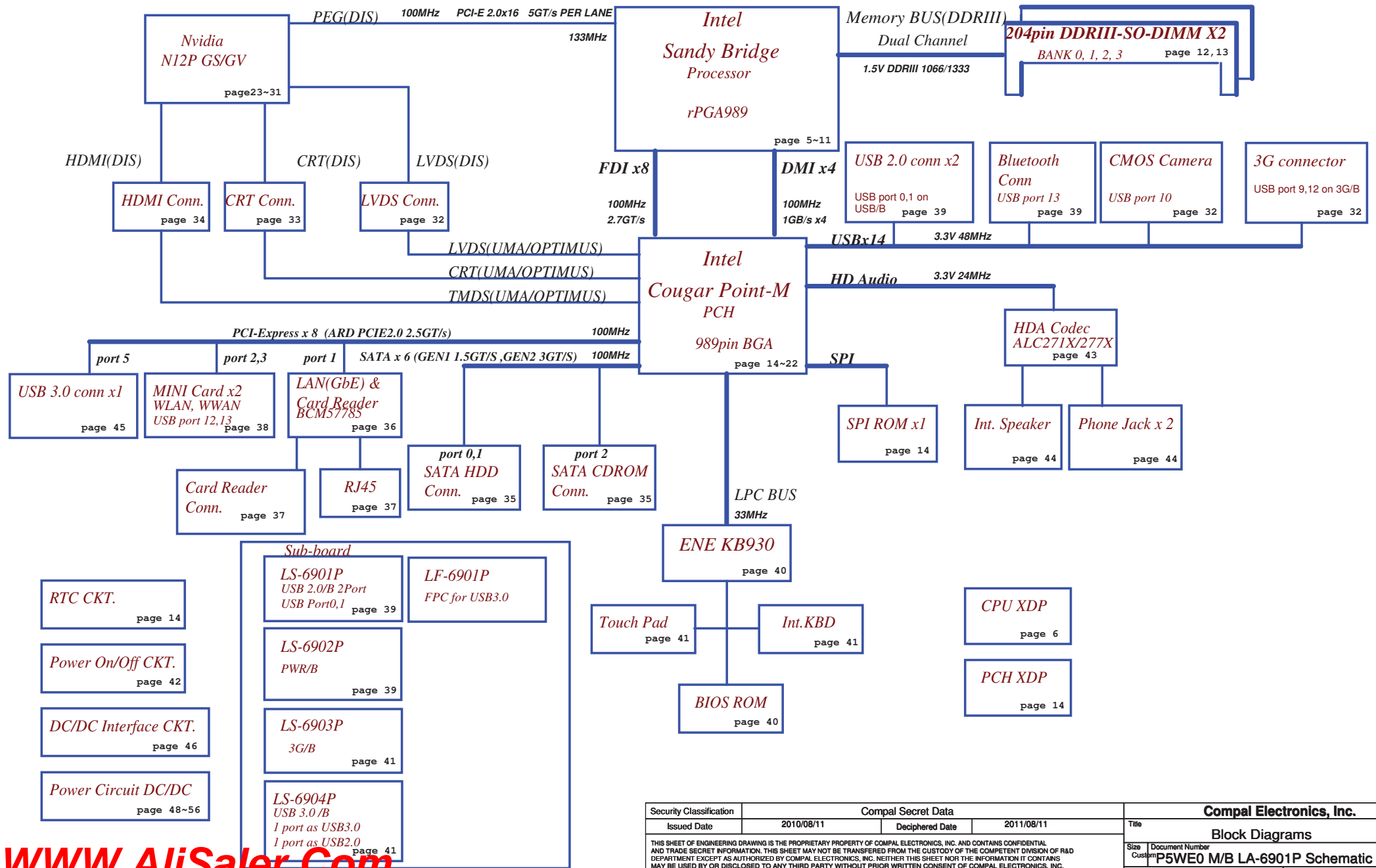
P5WE0 M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
Nvidia N12P GS/GV

2010-08-11

REV : 0 . 1

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2010/08/11	Deciphered Date	2011/08/11	Title	Cover Page	
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				Custom	P5WE0 M/B LA-6901P Schematic	
				Date	Friday, August 27, 2010	Sheet 1 of 59



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

3G & BT & USB30 & USB20 Config

3G SKU: 3G@ **USB30 SKU:** USB30@ **OPTIMUS SKU:** OPT@
BT SKU: BT@ **USB20 SKU:** USB20@ **Non-OPTIMUS SKU:** NOPT@
LAN Chip A0 version: A0@
LAN chip B0 Version: B0@

BOM Config

UMA Only: BT@/3G@/USB30@/UMA@/UMAO@/NOPT@/A0@
OPTIMUS: BT@/3G@/USB30@/UMA@/DIS@/X76@/OPT@/A0@
DIS Only: BT@/3G@/USB30@/DISO@/DIS@/X76@/NOPT@/A0@

VRAM BOM Config

X76*BOL01:** Samsung
X76*BOL02:** Hynix

VRAM P/N :

Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

EVT
DVT
PVT
Pre-MP

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

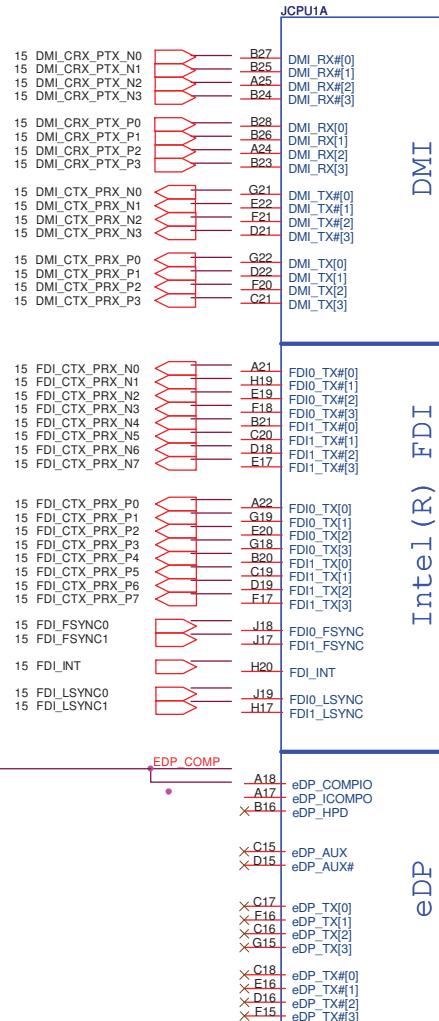
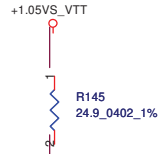
BTO Item	BOM Structure
UMA Only	UMAO@
UMA with OPTIMUS	UMA@
Dis with OPTIMUS	DIS@
DIS Only	DISO@
OPTIMUS	OPT@
Non-OPTIMUS	NOPT@
3G	3G@
Blue Tooth	BT@
USB2.0	USB20@
USB3.0	USB30@
VRAM	X76@
Connector	CONN@
Unpop	@
LAN Chip A0 version	A0@
LAN Chip B0 version	B0@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB/B (Right Side)
		2	USB 2.0 & USB3.0 Conn.
	UHCI1	3	
		4	
		5	
EHCI2	UHCI2	6	
		7	
		8	Mini Card 1(WLAN)
	UHCI3	9	3G/B(WWAN)
		10	Camera
		11	Mini Card 2(Reserved)
	UHCI6	12	SIM Card (3G/B)
		13	Blue Tooth

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Issued Date	2010/08/11	Deciphered Date	2011/08/11	Notes List		
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				Customer	P5WE0 M/B LA-6901P Schematic	0.1
				Date:	Friday, August 27, 2010	Sheet 3 of 59

eDP_COMPFIO and ICOMPO signals should be shorted near balls,
Trace Width for EDP_COMPFIO=4mils,
EDP_ICOMPO=12mils,
and both length less than 500 mils...
should not be left floating
,even if disable eDP function...

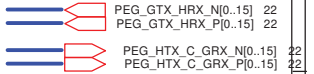


Sandy Bridge_rPGA_Rev0p61
CONN@

PCI EXPRESS* - GRAPHICS

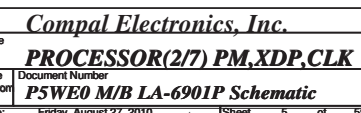


PEG_ICOMPI and PEG_RCOMPO signals should be shorted and routed,
max length = 500 mils,trace width=4mils
PEG_ICOMPO signals should be routed with - max
length = 500 mils,trace width=12mils
spacing =15mils

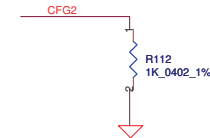


Typ- suggest 220nF. The change in AC capacitor
value from 100nF to 220nF is to enable
compatibility with future platforms having PCIe
Gen3 (8GT/s)

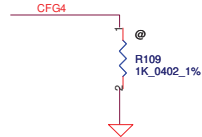
Security Classification		Compal Secret Data		Title	
Issued Date	2010/08/11	Deciphered Date	2011/08/11	PROCESSOR(1/7) DMI,FDI,PEG	
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				Date:	Friday, August 27, 2010
				Sheet	4 of 59



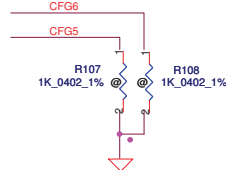
CFG Straps for Processor



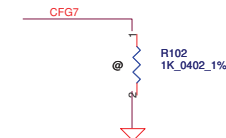
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	<p>1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>* 0: Lane Reversed</p>



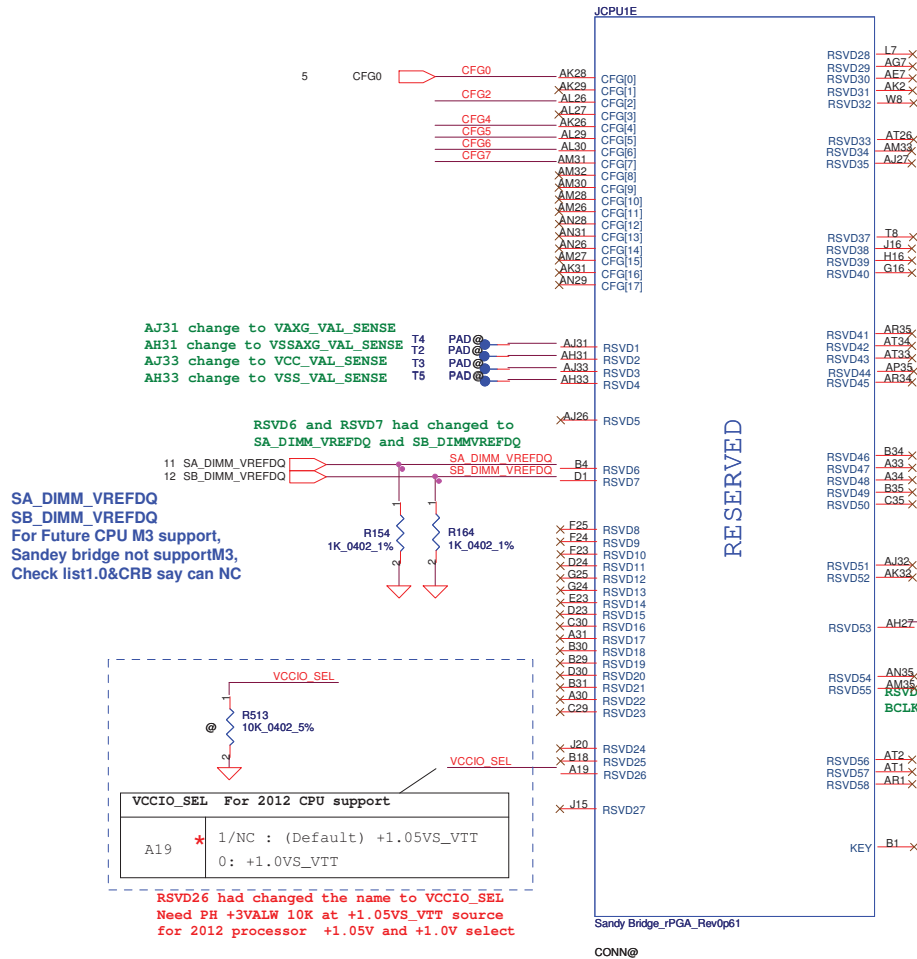
Display Port Presence Strap	
CFG4	<p>* 1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>



PCIe Port Bifurcation Straps	
CFG[6:5]	<p>* 11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</p> <p>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled</p>

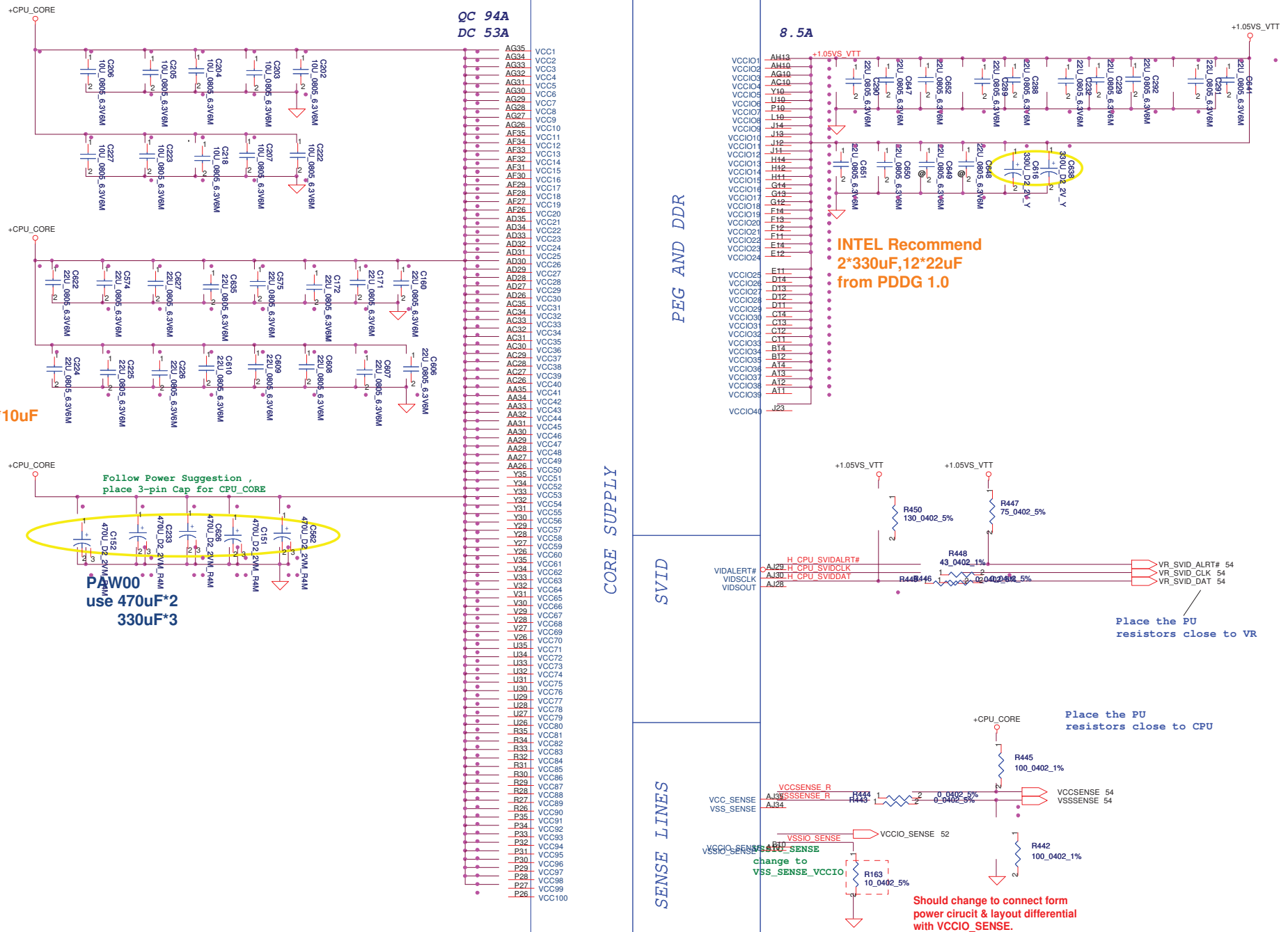


PEG DEFER TRAINING	
CFG7	<p>1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>



Sandy Bridge_rPGA_Rev0p61
CONN@

JCPU1F



**INTEL Recommend
4*470uF,16*22uF and 10*10uF
from PDDG 1.0**

PAW00 use 470uF*2
330uF*3

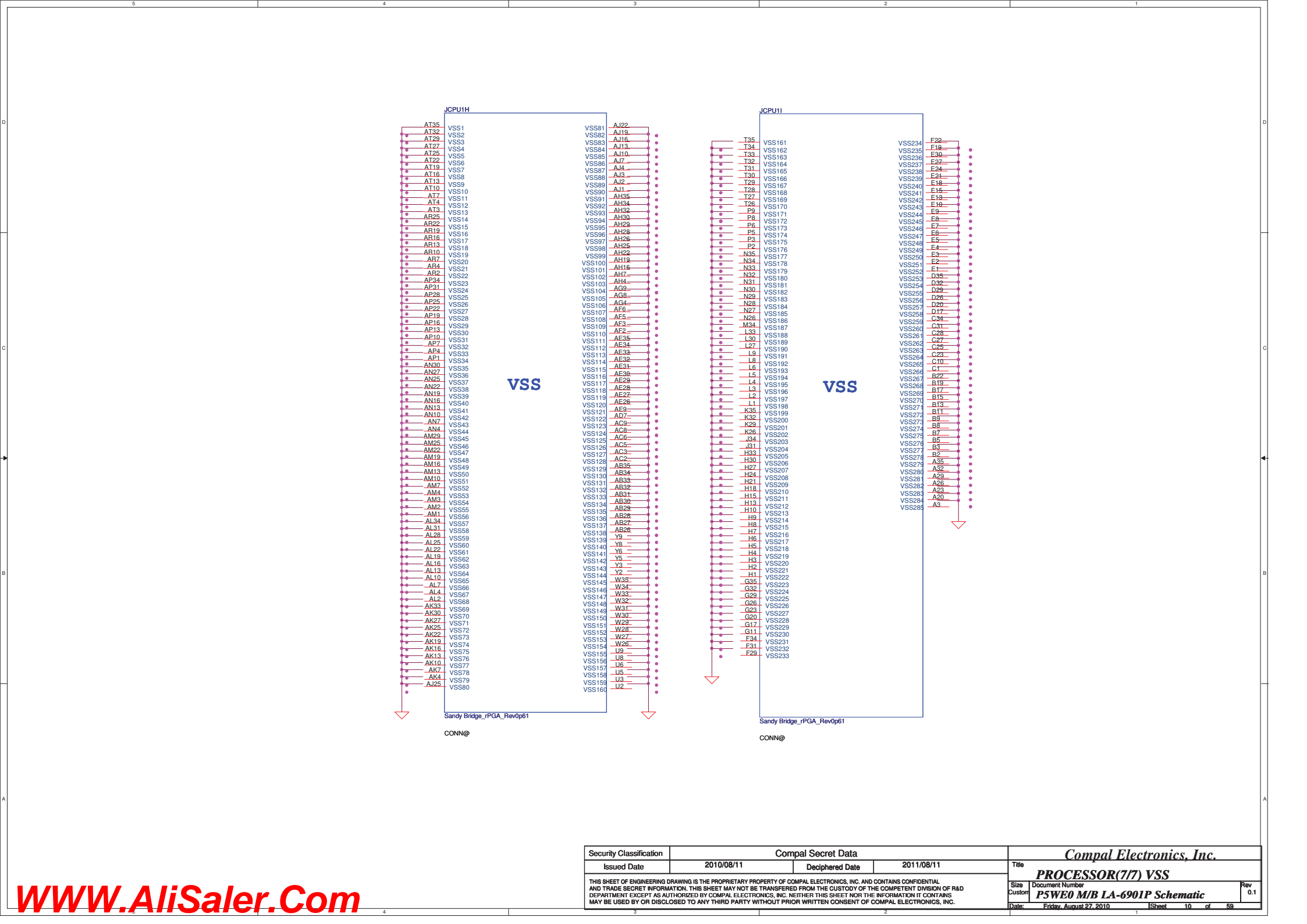
- INTEL Recommend
- 2*330uF,12*22uF
- from PDDG 1.0

Place the PU
resistors close to VR

Place the PU
resistors close to CPU

Should change to connect form power circuit & layout differential with VCCIO_SENSE.

Security Classification		Compal Secret Data		Sandy Bridge - PGA_Rev0p61 <i>Compal Electronics, Inc.</i>	
Issued To	2010/08/11	Deciphered Date	2011/08/11	Title PROCESSOR(5/7) PWR,BYPASS	
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				Custom	0.1
				Date: Friday, August 27, 2010 Sheet 8 of 59	
				P5WE0 M/B LA-6901P Schematic	



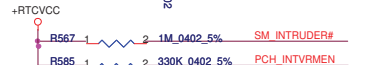
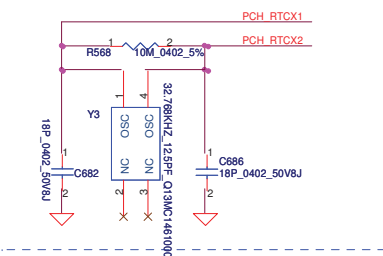






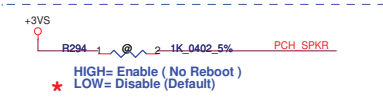
— *Journal of the American Medical Association*, 1997

Date:	Friday, August 22, 2010	Score:	11	0	59
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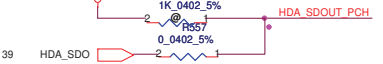


INTVRMEN
 * H : Integrated VRM enable
 L : Integrated VRM disable

(INTVRMEN should always be pull high.)



HIGH= Enable (No Reboot)
 LOW= Disable (Default)

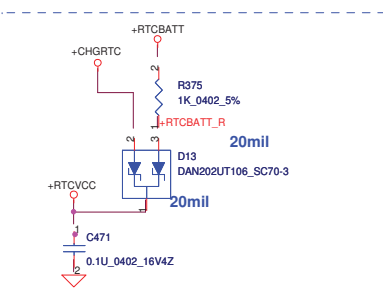
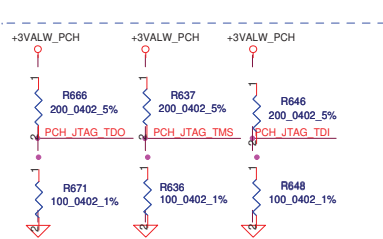
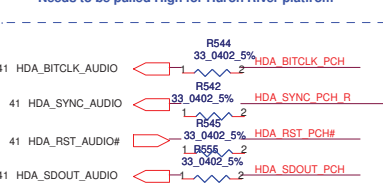


HDA_SDO as Capella ME override (GPIO33)
 ME debug mode, this signal has a weak internal PD
 Low = Disabled (Default)
 High = Enabled [Flash Descriptor Security Override]

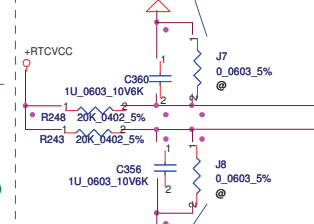


This signal has a weak internal pull-down

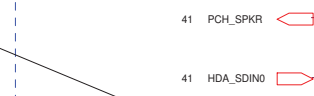
On Die PLL VR Select is supplied by 1.5V when smaped high 1.8V when sampled low Needs to be pulled High for Huron River platform



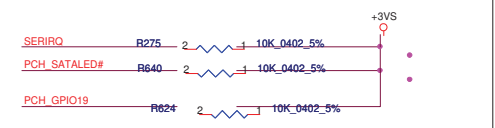
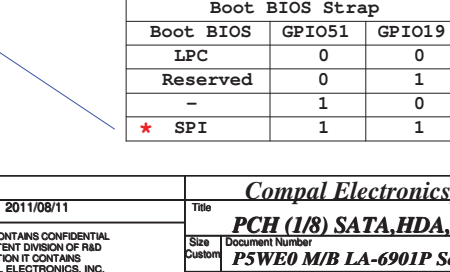
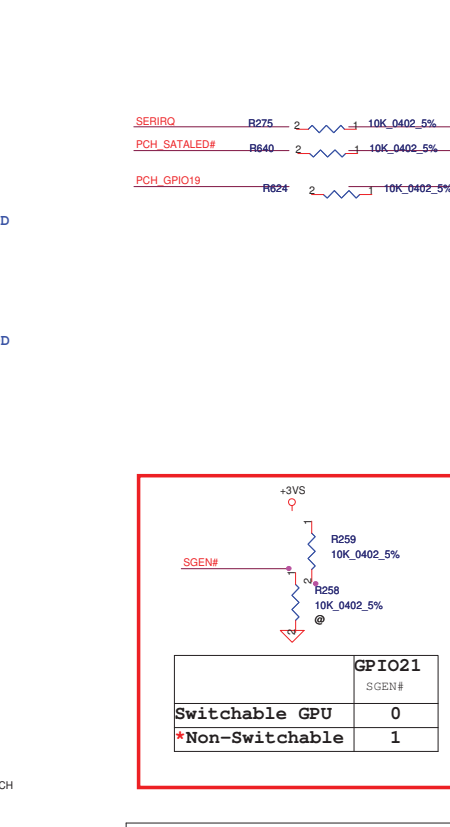
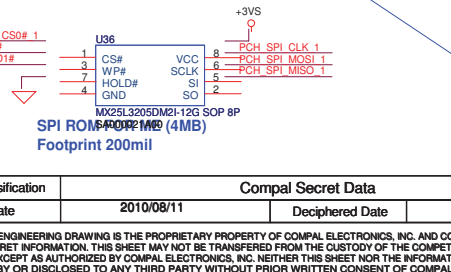
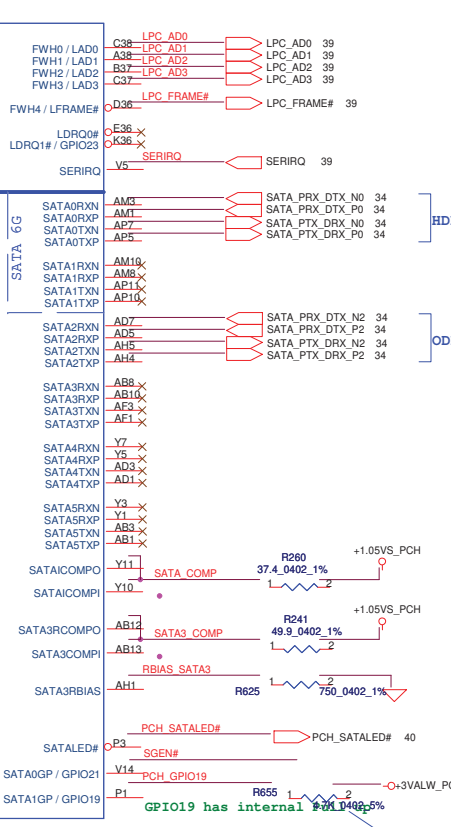
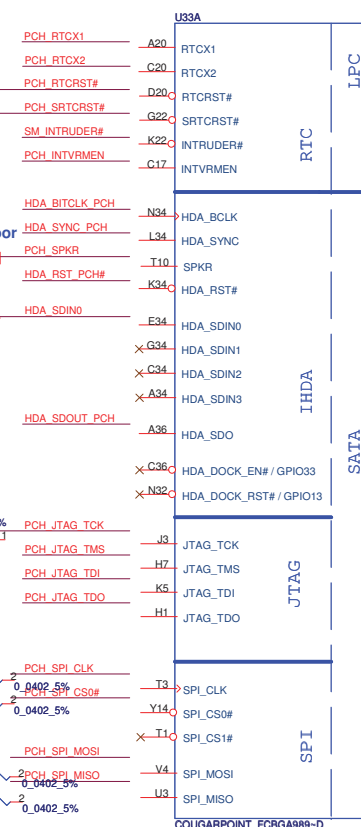
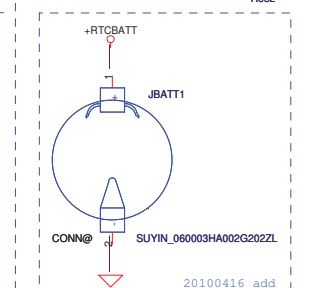
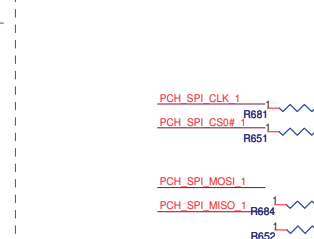
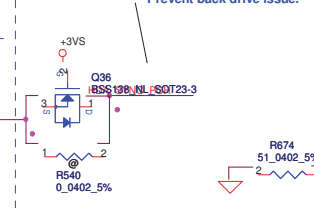
RTCRST close RAM door



SRTCST close RAM door

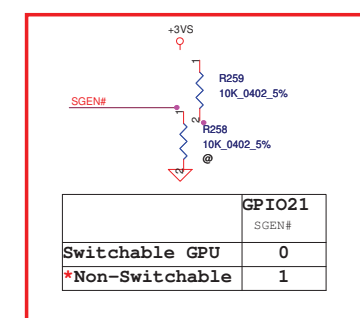


Prevent back drive issue.



PCH_SATALED# R640 2 10K_0402_5%

PCH_GPIO19 R624 2 10K_0402_5%



GPIO21 SGEN#

Switchable GPU 0

*Non-Switchable 1

GPIO21 SGEN#

Switchable GPU 0

*Non-Switchable 1

GPIO21 SGEN#

Switchable GPU 0

*Non-Switchable 1

GPIO21 SGEN#

GPIO21 SGEN#

Switchable GPU 0

*Non-Switchable 1

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GPIO21 SGEN#

Switchable GPU 0

*Non-Switchable 1

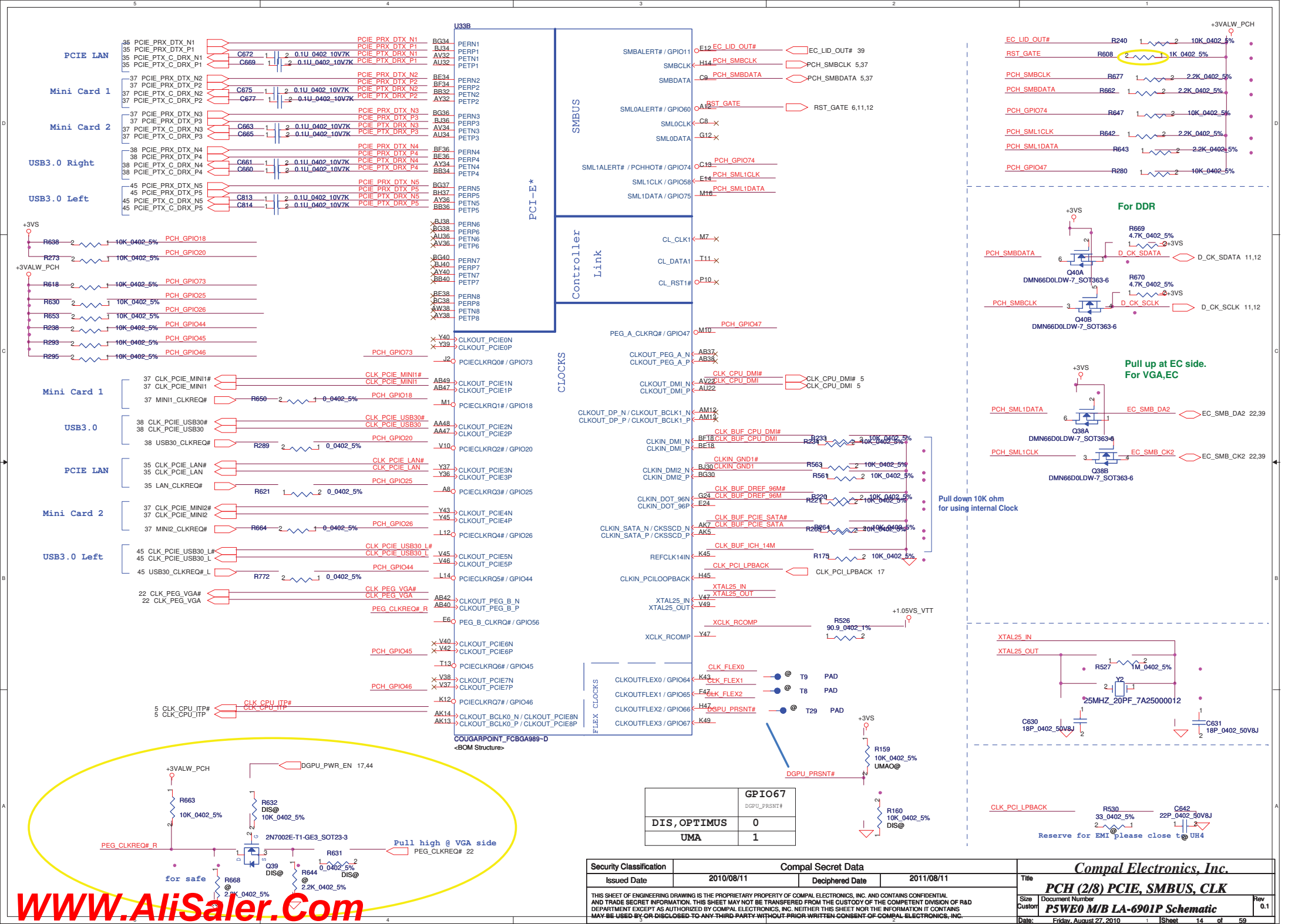
GPIO21 SGEN#

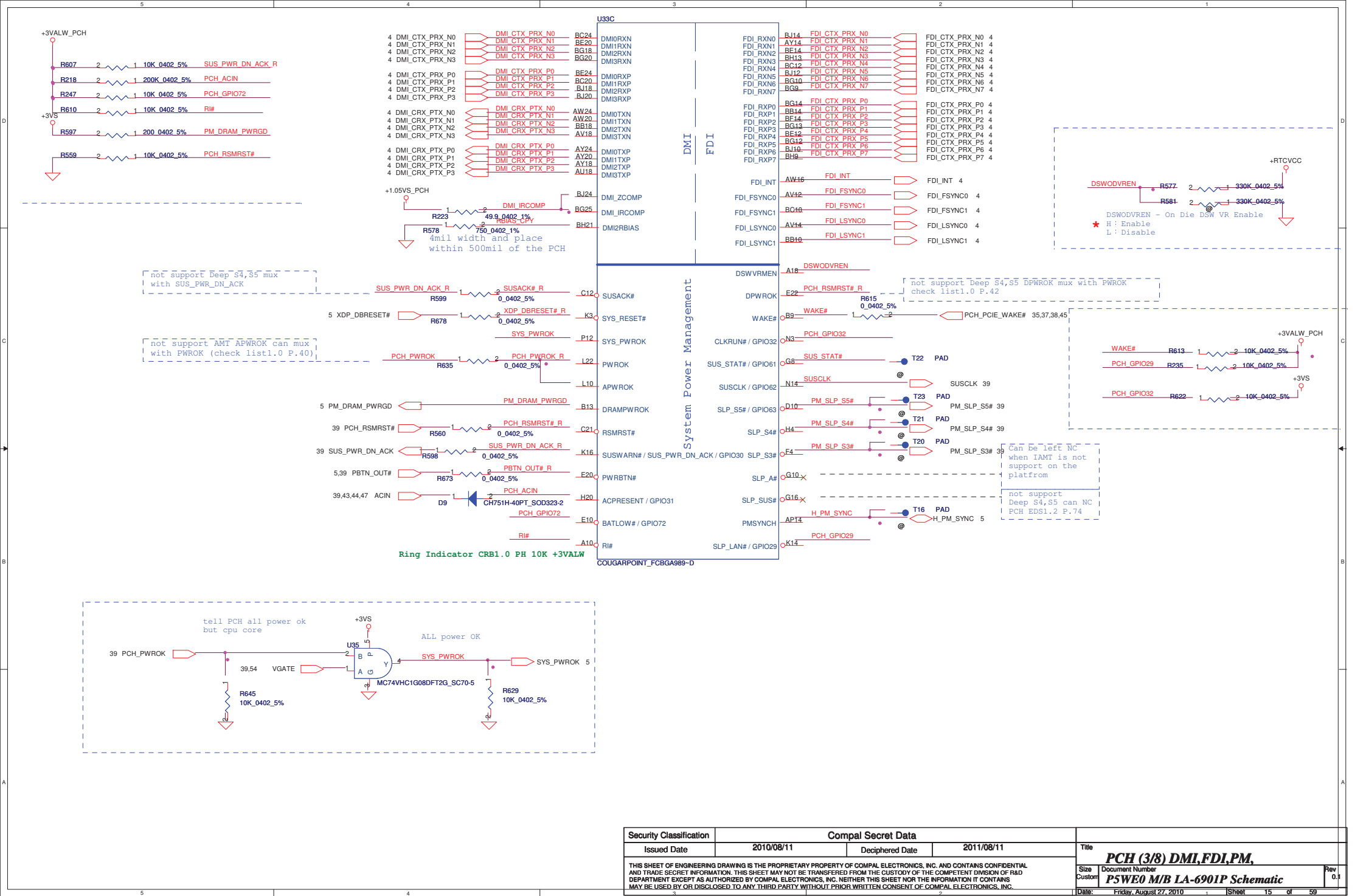
Switchable GPU 0

*Non-Switchable 1

GPIO21 SGEN#

Switchable GPU 0





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Date				Friday, August 27, 2010	Sheet 15 of 59

22.39 ENBKL ENBKL R532 2 0.0402 5% IGPU_BKLT_EN
UMA@

31 PCH_LCD_CLK
31 PCH_LCD_DATA



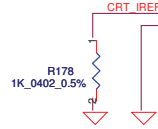
Pull high at LVDS conn side.

31 PCH_TXCLK-
31 PCH_TXCLK+
31 PCH_TXOUT0-
31 PCH_TXOUT1-
31 PCH_TXOUT2-
31 PCH_TXOUT0+
31 PCH_TXOUT1+
31 PCH_TXOUT2+

32 PCH_CRT_B
32 PCH_CRT_G
32 PCH_CRT_R

32 PCH_CRT_CLK
32 PCH_CRT_DATA

32 PCH_CRT_HSYNC
32 PCH_CRT_VSYNC



U33D

L_BKLTEN
L_VDD_EN
L_BKLTCTL
T40
K47
T45
P39
L_CTRL_CLK
L_CTRL_DATA

LVDS_IBG
LVDS_VBG
AE37
AE36
AE48
AE47
LVDS_VREFH
LVDS_VREFL

LVDSA_CLK#
LVDSA_CLK
LVDSA_DATA#0
LVDSA_DATA#1
LVDSA_DATA#2
LVDSA_DATA#3
LVDSA_DATA0
LVDSA_DATA1
LVDSA_DATA2
LVDSA_DATA3

LVDSB_CLK#
LVDSB_CLK
LVDSB_DATA#0
LVDSB_DATA#1
LVDSB_DATA#2
LVDSB_DATA#3
LVDSB_DATA0
LVDSB_DATA1
LVDSB_DATA2
LVDSB_DATA3

CRT_BLUE
CRT_GREEN
CRT_RED

CRT_DDC_CLK
CRT_DDC_DATA

CRT_HSYNC
CRT_VSYNC

DAC_IREF
CRT_IRTN

COUGARPOINT_FCBGA989-D

SDVO_TVCLKINN
SDVO_TVCLKINP
SDVO_STALLN
SDVO_STALLP
SDVO_INTN
SDVO_INTP

SDVO_CTRLCLK
SDVO_CTRLDATA

DDPB_AUXN
DDPB_AUXP
DDPB_HPD

DDPB_0N
DDPB_0P
DDPB_1N
DDPB_1P
DDPB_2N
DDPB_2P
DDPB_3N
DDPB_3P

DDPC_CTRLCLK
DDPC_CTRLDATA

DDPC_AUXN
DDPC_AUXP
DDPC_HPD

DDPC_0N
DDPC_0P
DDPC_1N
DDPC_1P
DDPC_2N
DDPC_2P
DDPC_3N
DDPC_3P

DDPD_CTRLCLK
DDPD_CTRLDATA

DDPD_AUXN
DDPD_AUXP
DDPD_HPD

DDPD_0N
DDPD_0P
DDPD_1N
DDPD_1P
DDPD_2N
DDPD_2P
DDPD_3N
DDPD_3P

SDVO_CTRLDATA strap pull high
at level shift page

P38 SDVO_SCLK
M39 SDVO_SDATA

AT49
AT47
AT46
PCH_DPB_HPD

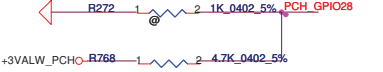
PCH_DPB_N0
PCH_DPB_P0
PCH_DPB_N1
PCH_DPB_P1
PCH_DPB_N2
PCH_DPB_P2
PCH_DPB_N3
PCH_DPB_P3

HDMI D2
HDMI D1
HDMI D0
HDMI CLK

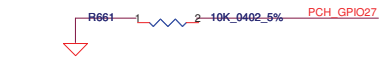
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				Date	Friday, August 27, 2010
				Sheet	16 of 59
				Rev	0.1

GPIO28 HDA_SYNC PH (PLL =+1.5VS)
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

★ H: On-Die voltage regulator enable
L: On-Die PLL Voltage Regulator disable

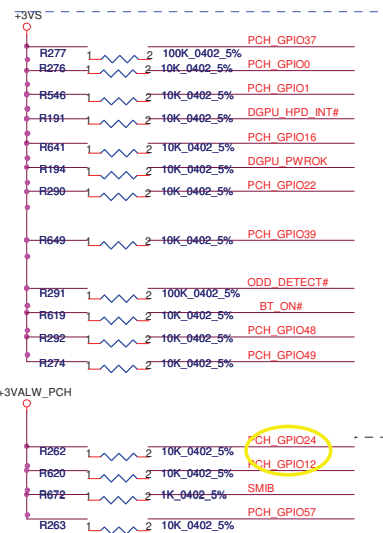


Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND Check list1.0 P.70

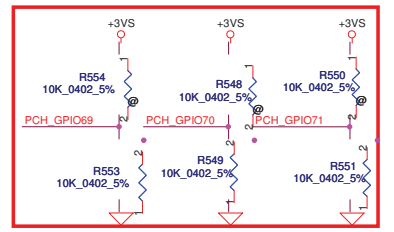
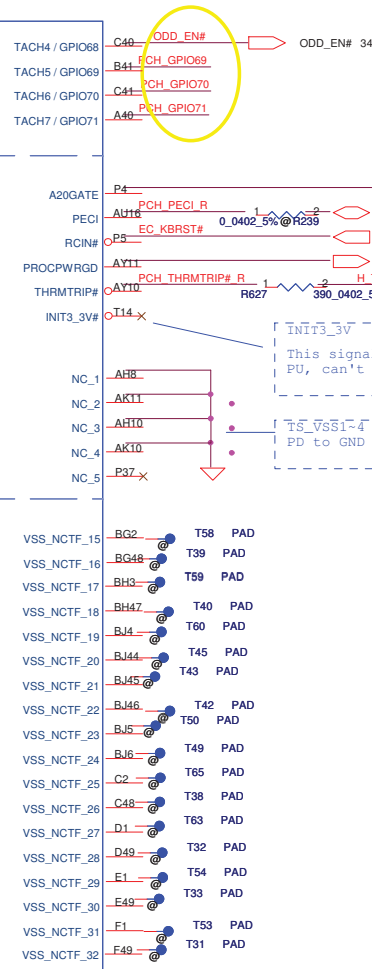
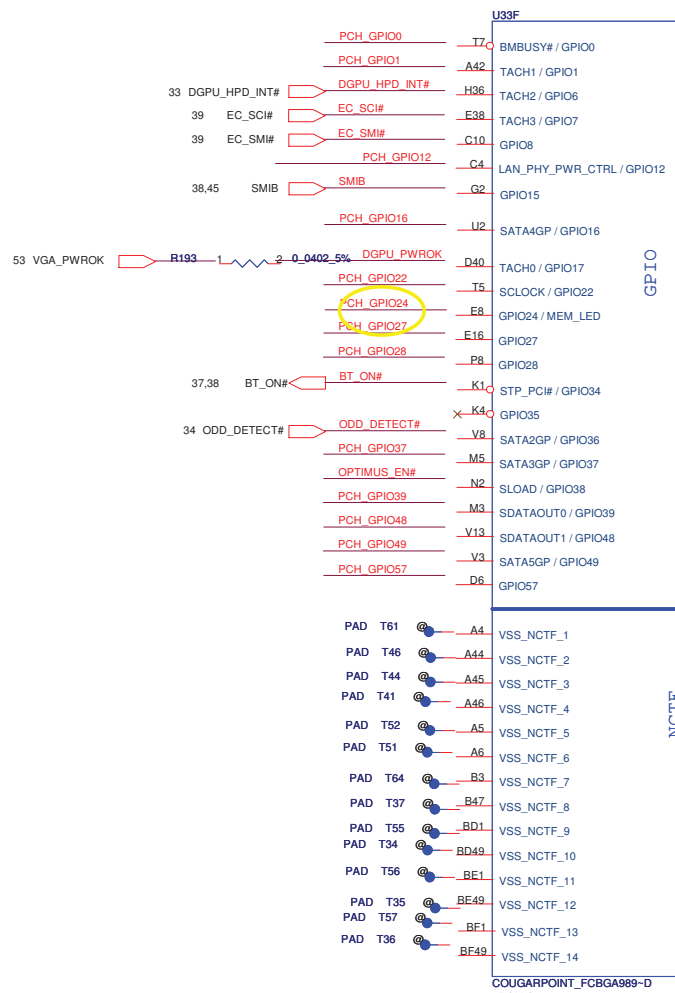


3VS

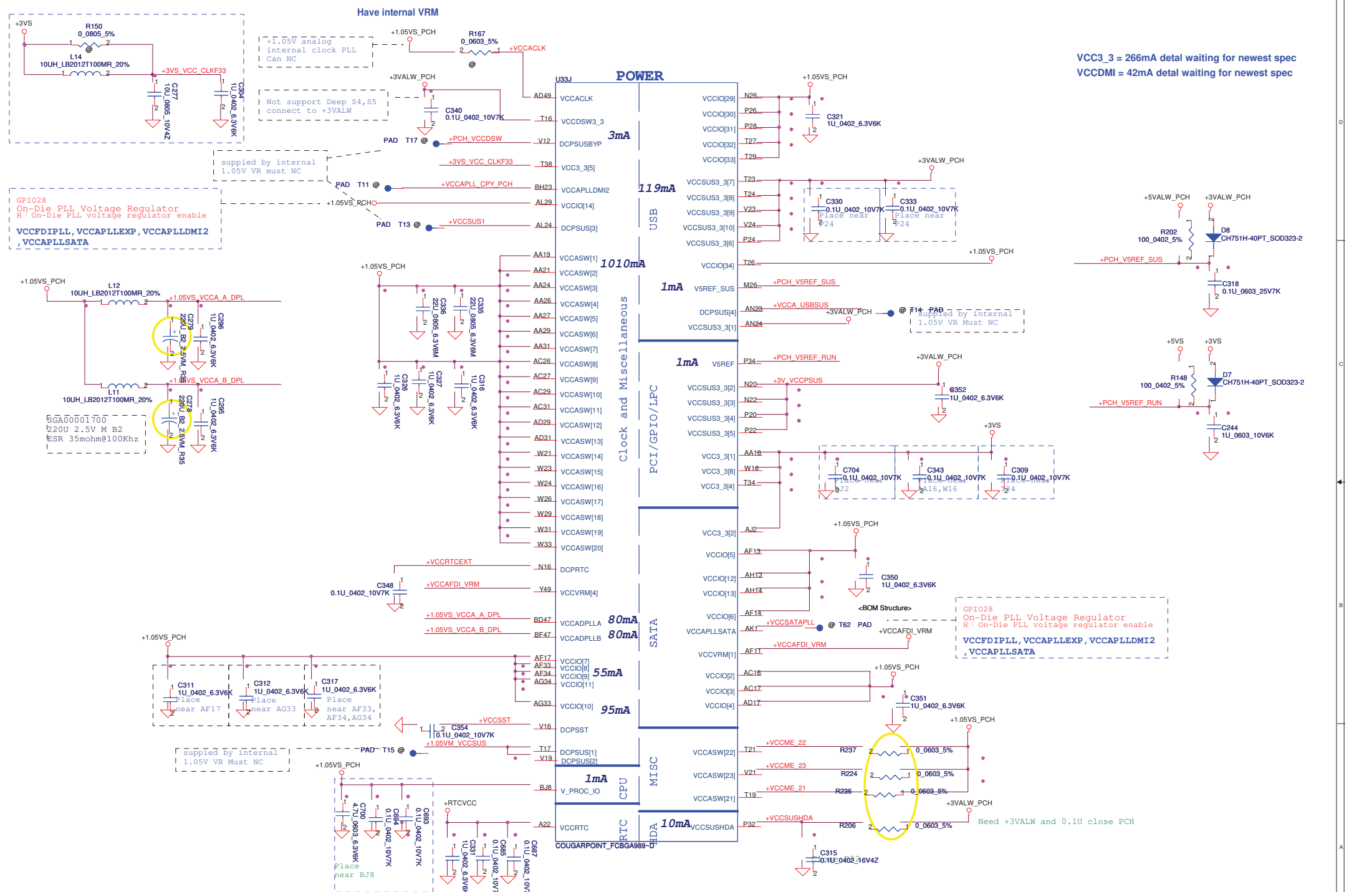
	GPIO38
OPTIMUS	0
Non-OPTIMUS	1



Gpio24 Unmultiplexed
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.
CRB1.0 PH10K to +3VALW

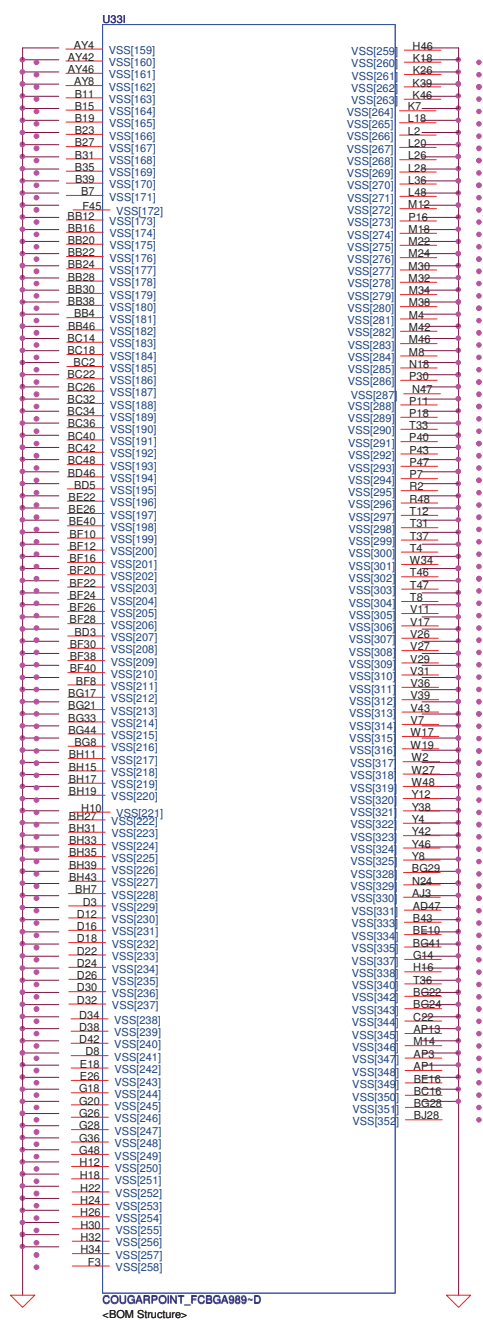
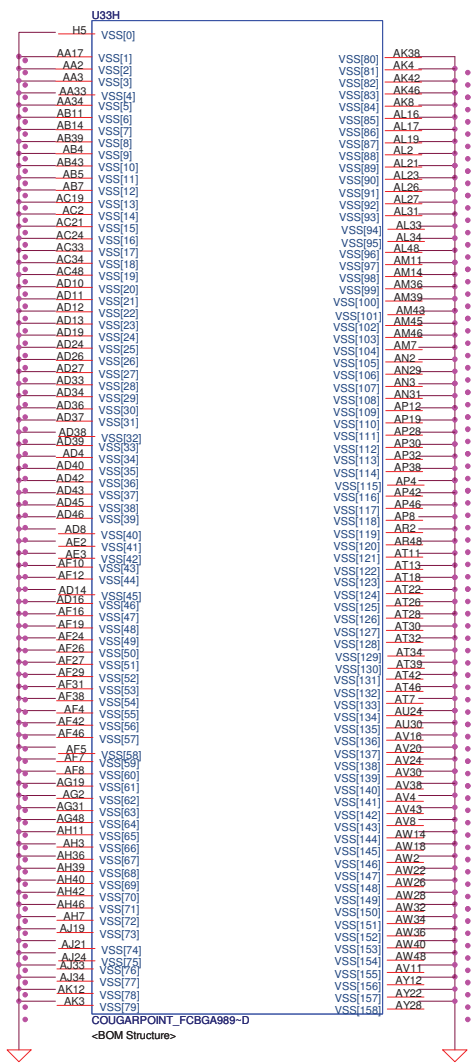


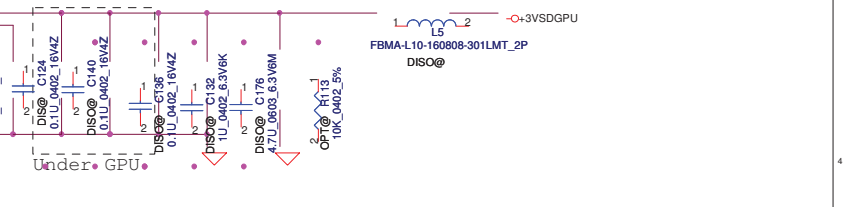
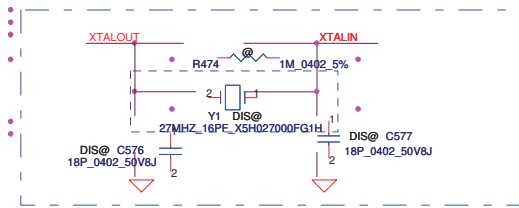
Project ID	GPIO69	GPIO70	GPIO71
★ P5WE0	0	0	0
P7YE0	0	0	0
x	0	1	0
x	0	1	1
x	1	0	0
x	0	0	1
x	0	1	0
x	0	1	1
x	1	0	0
x	1	0	1
x	1	1	0
x	1	1	1



VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

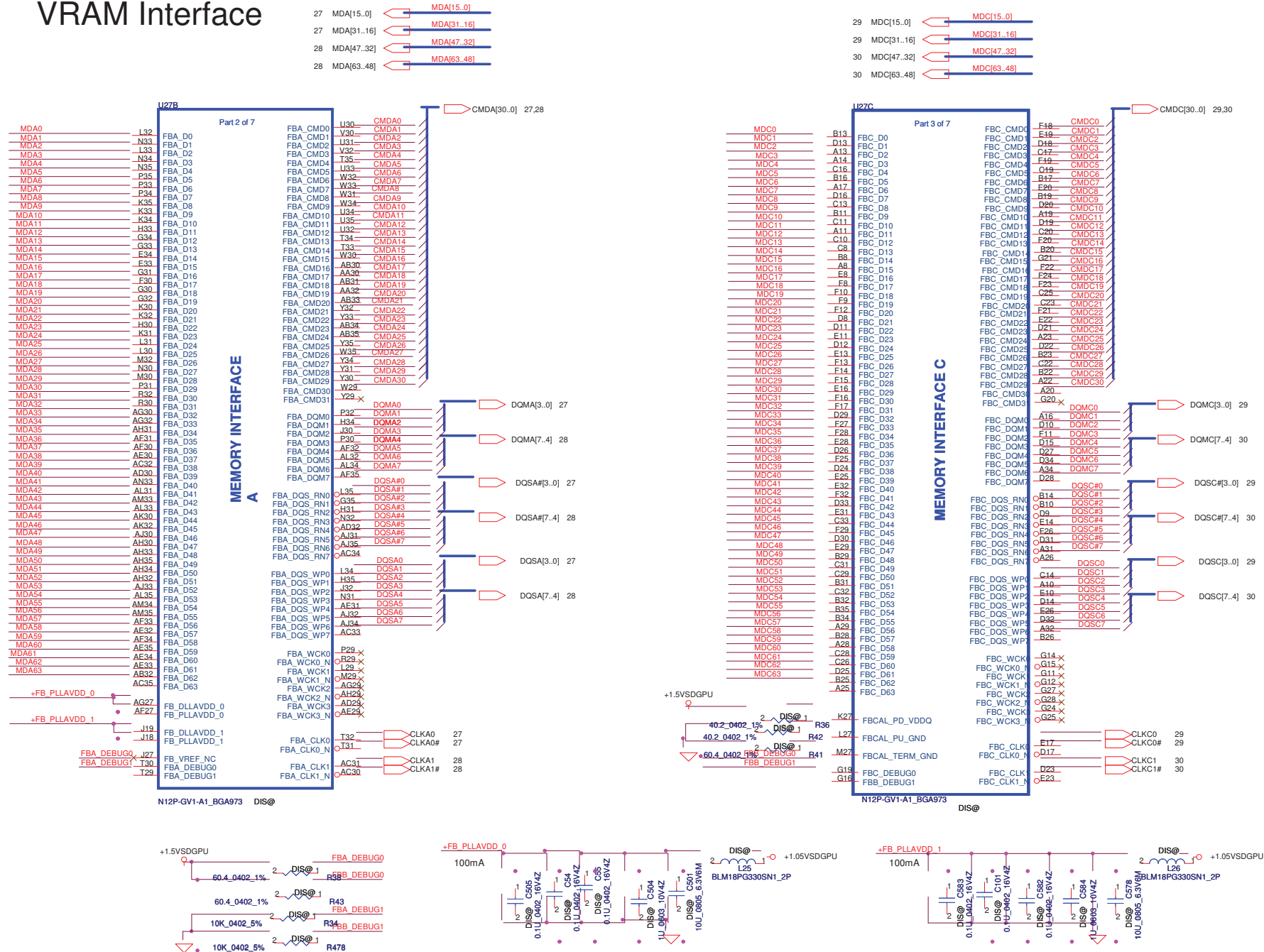
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				Date	Friday, August 27, 2010
				Sheet	20 of 59





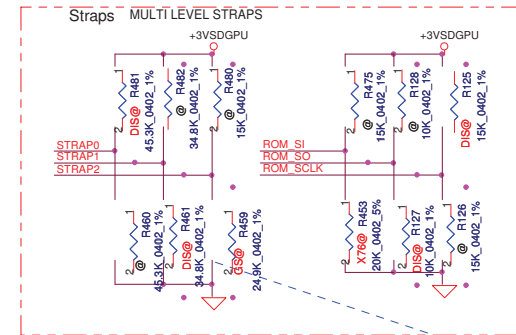
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				Custom	01
				Document Number	
				P5WE M/B LA-6901P Schematic Date: Friday, August 27, 2010 11:51 AM Sheet 22 of 59	

VRAM Interface




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					N12P VRAM 2/9
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Size		Document Number		Rev	
Custom		P5WE0 M/B LA-6901P Schematic		0.1	
Date:		Friday, August 27, 2010		Sheet 23 of 59	

The diagram shows the electrical connections for the STRAP4 and STRAP3 signals. STRAP4 is connected to the PGOOD signal through a 10K_0402_5% resistor (R778). STRAP3 is connected to a 40.2K_0402_1% resistor (R779). Both signals are connected to a +3VSDGPU supply through a 10K_0402_5% resistor (R774 for STRAP4 and R775 for STRAP3). The STRAP4 path also includes a 10K_0402_5% resistor (R776) and a 10K_0402_5% resistor (R777) connected to ground.

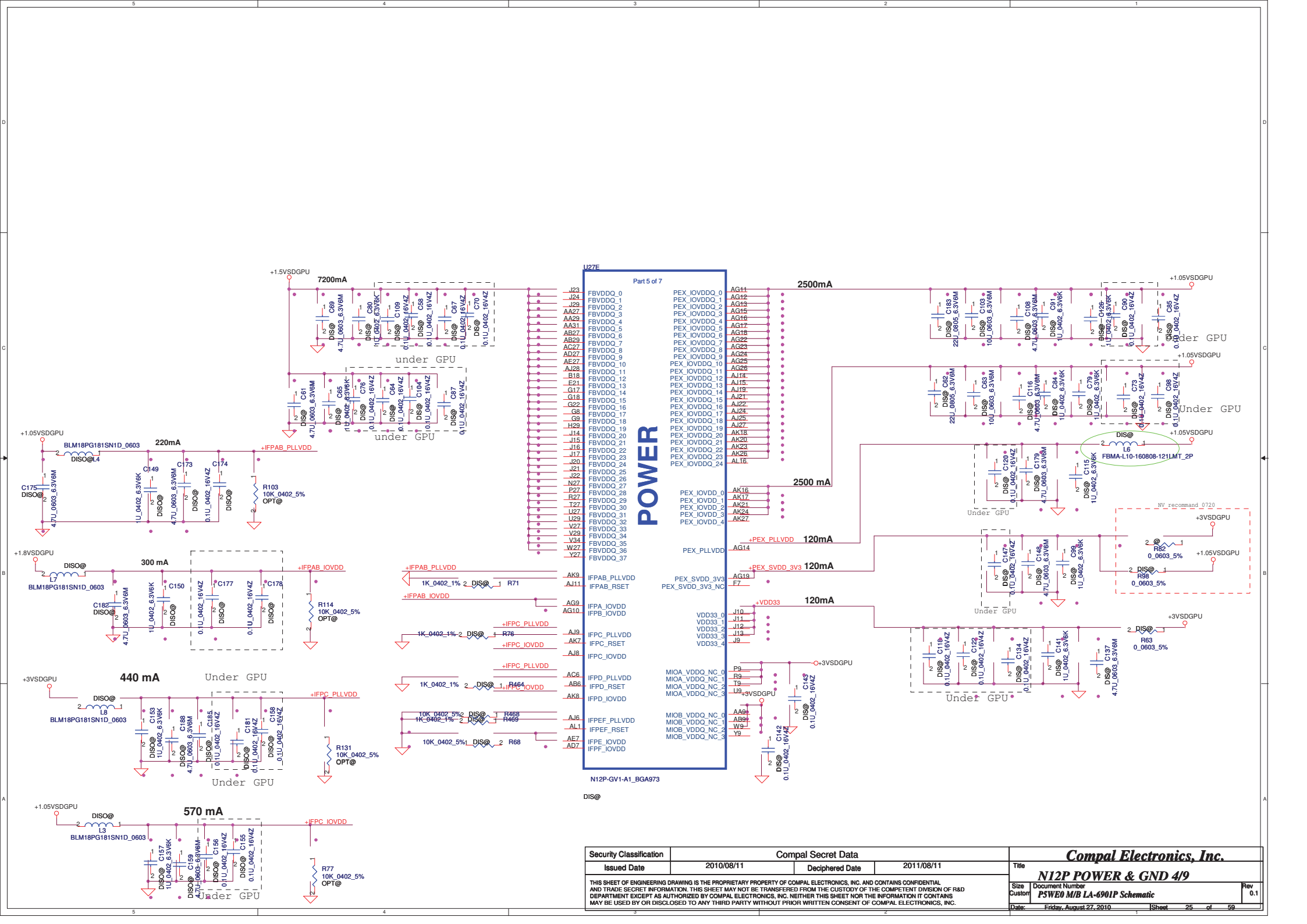


N12P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA000035700	H 45K	L 35K	L 25K	L 20K	L 10K	H 15K
64MX16 Hynix SA000032400	H 45K	L 35K	L 25K	L 15K	L 10K	H 15K
128MX16 Samsung	H 45K	L 35K	L 25K	L 45K	L 10K	H 15K
128MX16 Hynix SA00003VS10	H 45K	L 35K	L 25K	L 35K	L 10K	H 15K

GV@ R459
45K 0402 1%

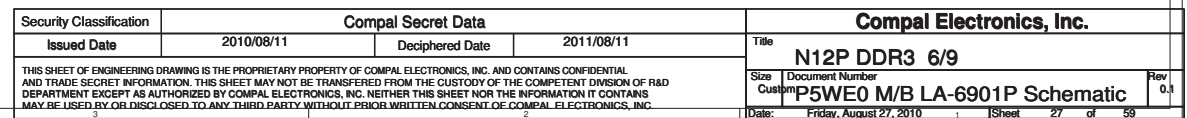


Strap 2 for GV1,
Pull low 45K Ohm

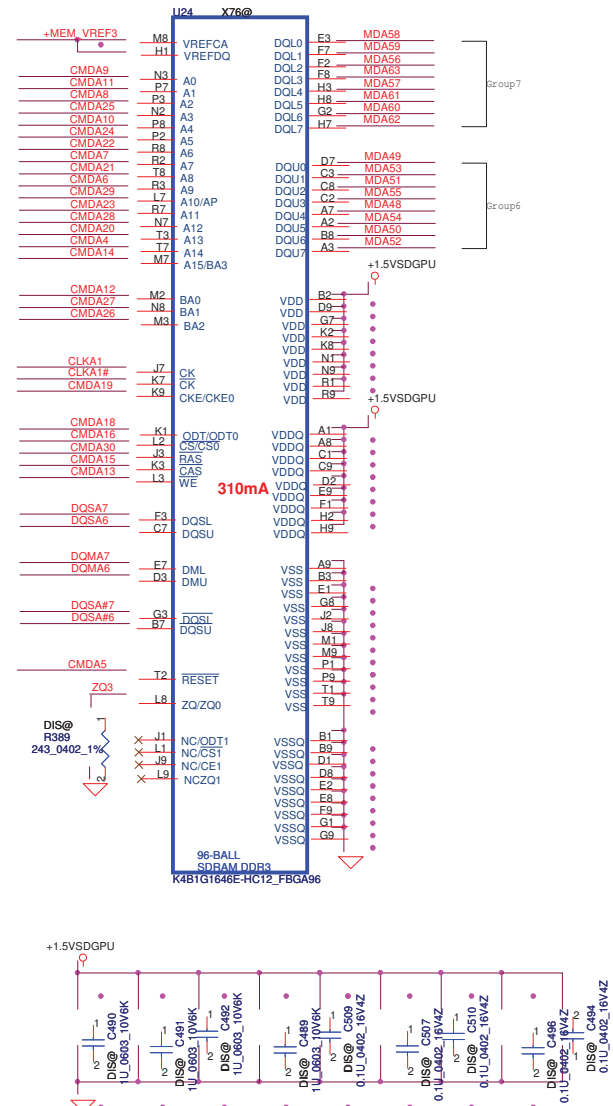
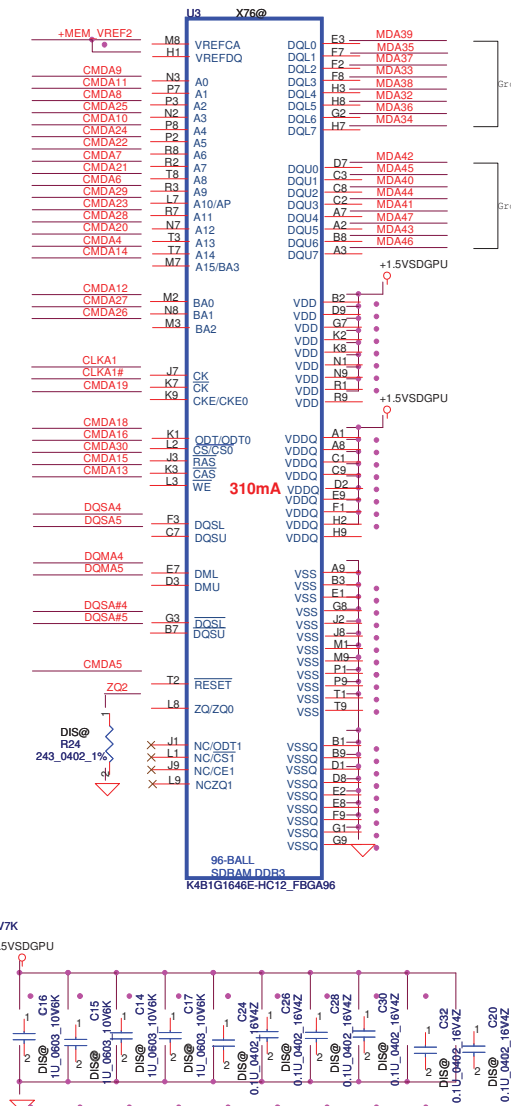


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				N12P POWER & GND 4/9					
				Size		Document Number		Rev	
				Custom		PSWEO M/B LA-6901P Schematic		0.1	
				Date		Friday, August 27, 2010		Sheet 25 of 59	

64Mx16 DDR3 *8==>1GB



64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

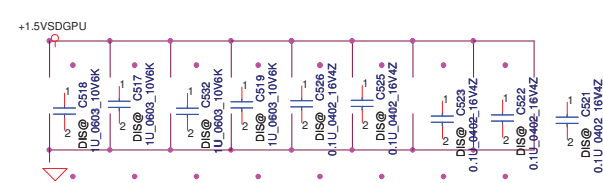
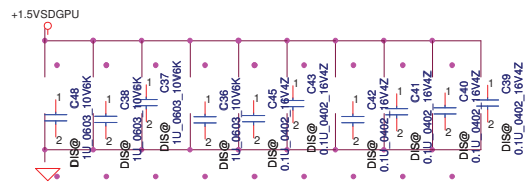
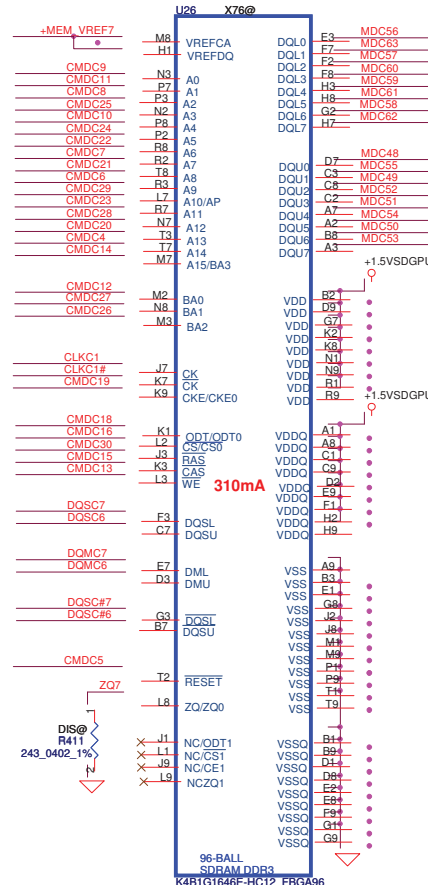
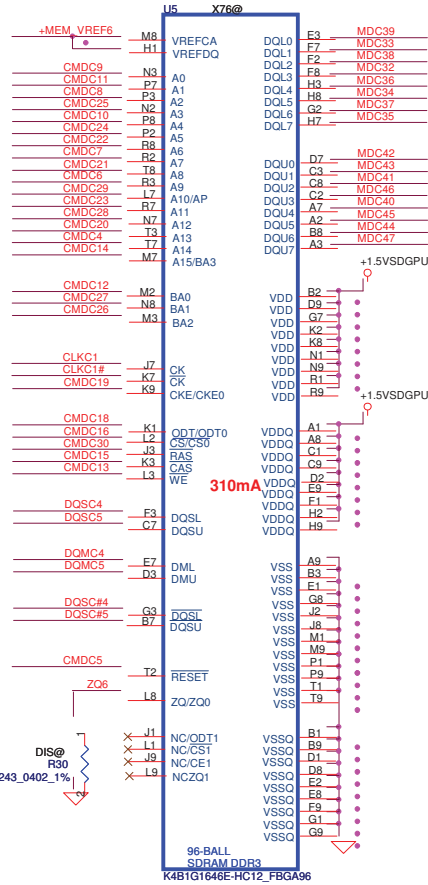
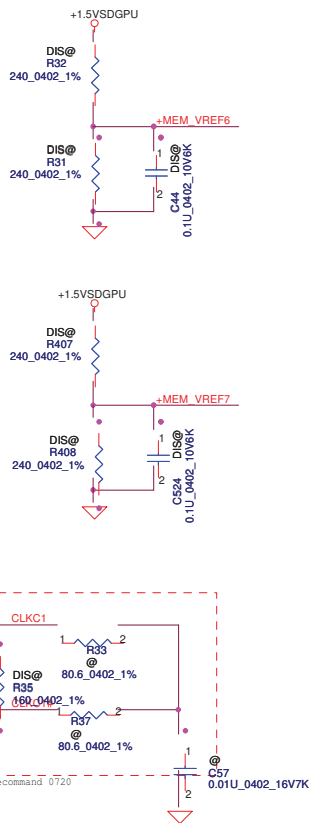
64Mx16 DDR3 *8==>1GB

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				Size	Document Number
				Customer	M5WE0 M/B LA-6901P Schematic
				Date:	Friday, August 27, 2010
				Sheet	29 of 59

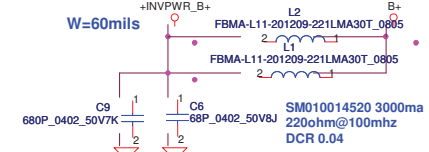
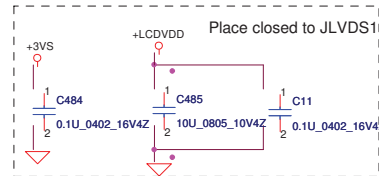
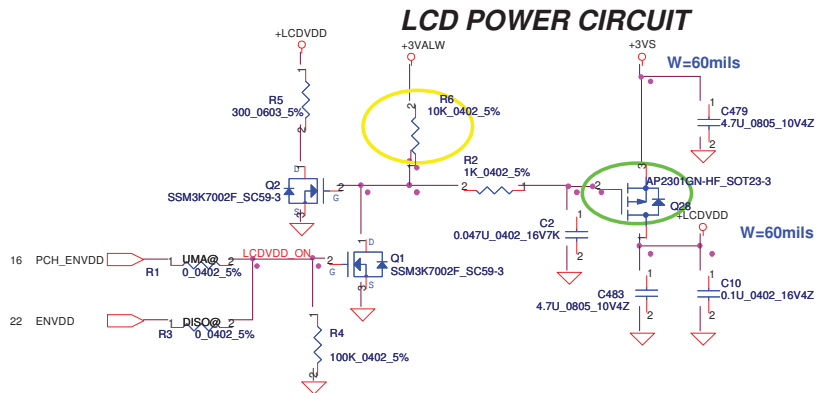
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

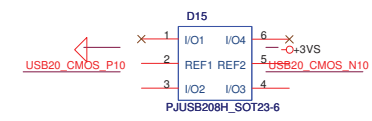
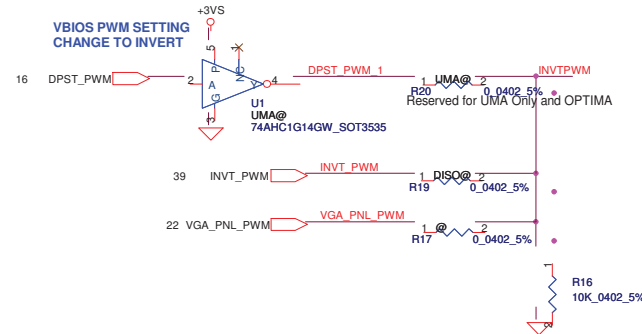
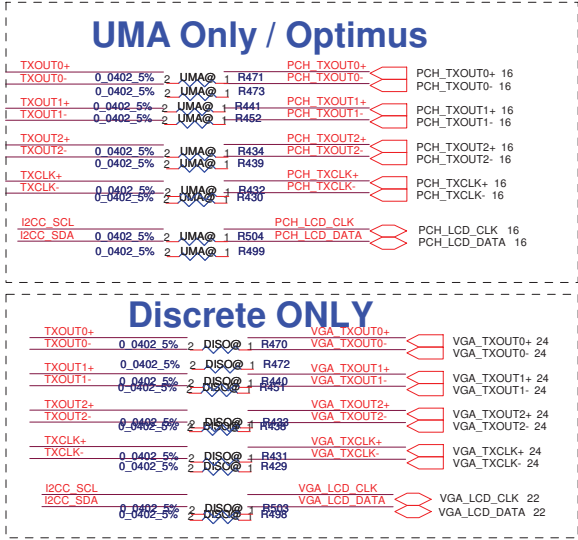
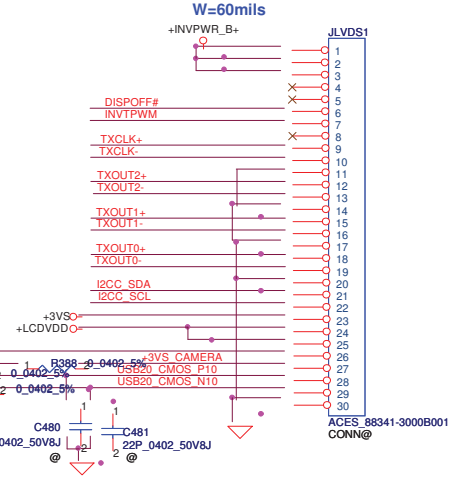
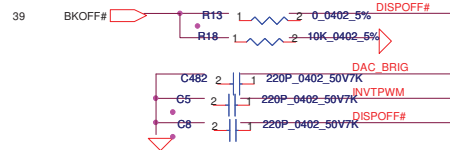
23.29 DOMC[7..0] \hookrightarrow DOMC[7..0]
 23.29 CMDC[30..0] \hookrightarrow CMDC[30..0]
 23.29 DQSC[7..0] \hookrightarrow DQSC[7..0]
 23.29 DQSC[7..0] \hookrightarrow DQSC[7..0]
 23.29 MDC[63..0] \hookrightarrow MDC[63..0]



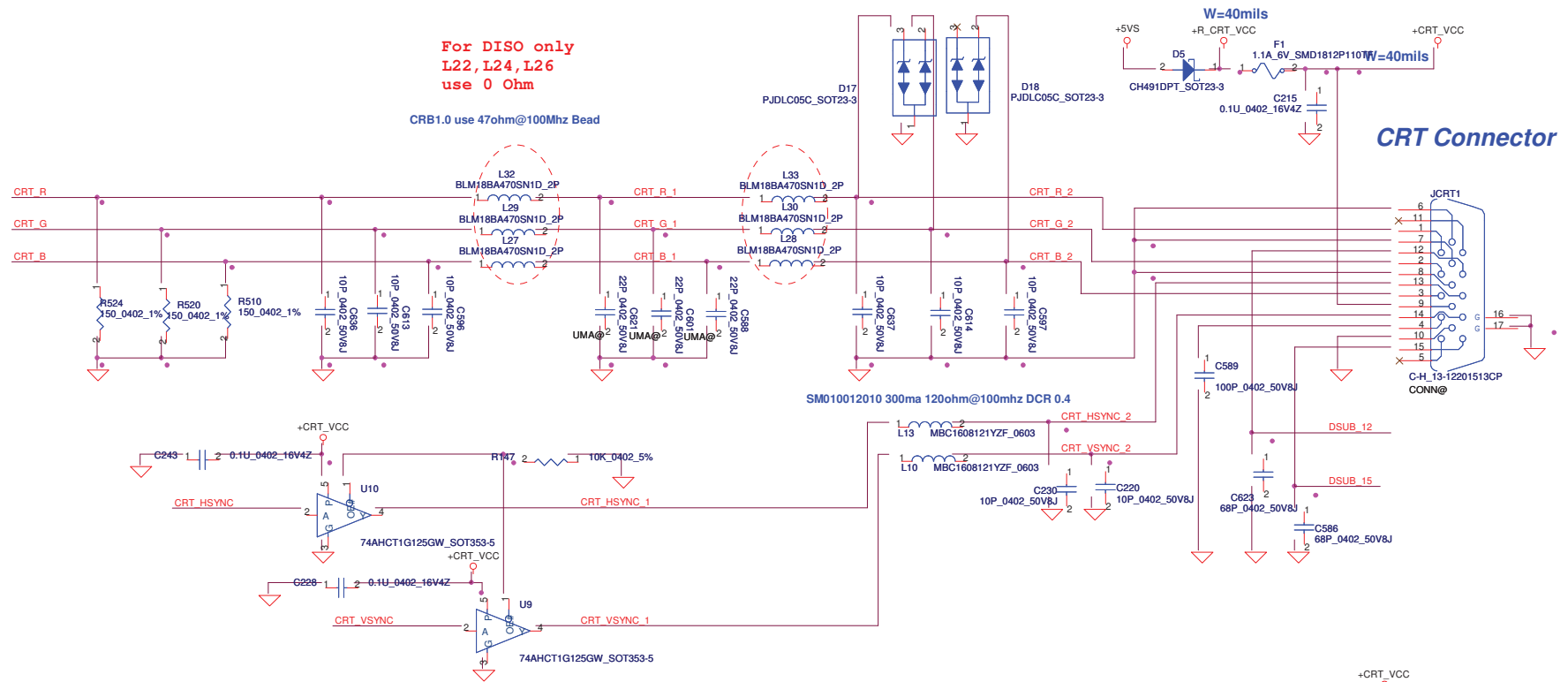
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH



LCD/LED PANEL Conn.



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Size		Document Number		Rev	
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Date		Friday, August 27, 2010		Sheet	
				31 of 59	



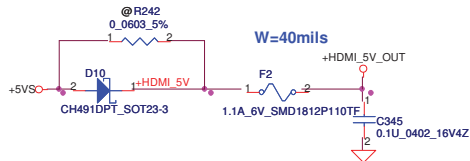
UMA Only / OPTIMUS

16	PCH_CRT_R	PCH_CRT_R	R420	UMA@	0_0402_5%	CRT_R
16	PCH_CRT_G	PCH_CRT_G	R424	UMA@	0_0402_5%	CRT_G
16	PCH_CRT_B	PCH_CRT_B	R422	UMA@	0_0402_5%	CRT_B
16	PCH_CRT_HSYNC	PCH_CRT_HSYNC	R428	UMA@	33_0402_5%	CRT_HSYNC
16	PCH_CRT_VSYNC	PCH_CRT_VSYNC	R426	UMA@	33_0402_5%	CRT_VSYNC
16	PCH_CRT_CLK	PCH_CRT_CLK	R506	UMA@	0_0402_5%	CRT_DDC_CLK
16	PCH_CRT_DATA	PCH_CRT_DATA	R501	UMA@	0_0402_5%	CRT_DDC_DATA

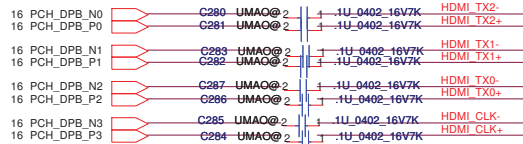
Discrete only

22	VGA_CRT_R	VGA_CRT_R	R419	DISO@	0_0402_5%	CRT_R
22	VGA_CRT_G	VGA_CRT_G	R423	DISO@	0_0402_5%	CRT_G
22	VGA_CRT_B	VGA_CRT_B	R421	DISO@	0_0402_5%	CRT_B
22	VGA_CRT_HSYNC	VGA_CRT_HSYNC	R427	DISO@	0_0402_5%	CRT_HSYNC
22	VGA_CRT_VSYNC	VGA_CRT_VSYNC	R425	DISO@	0_0402_5%	CRT_VSYNC
22	VGA_DDC_CLK	VGA_DDC_CLK	R505	DISO@	0_0402_5%	CRT_DDC_CLK
22	VGA_DDC_DATA	VGA_DDC_DATA	R500	DISO@	0_0402_5%	CRT_DDC_DATA

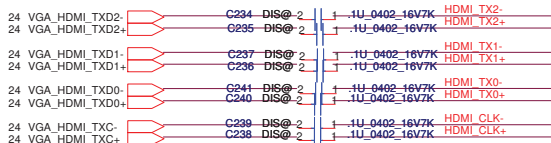
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Issued Date	2010/08/11	Deciphered Date	2011/08/11	CRT Connector	
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				Customer	P5WE0 M/B LA-6901P Schematic
				Date	Friday, August 27, 2010
				Sheet	32 of 59



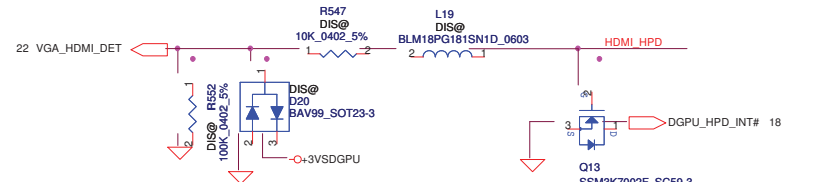
UMA



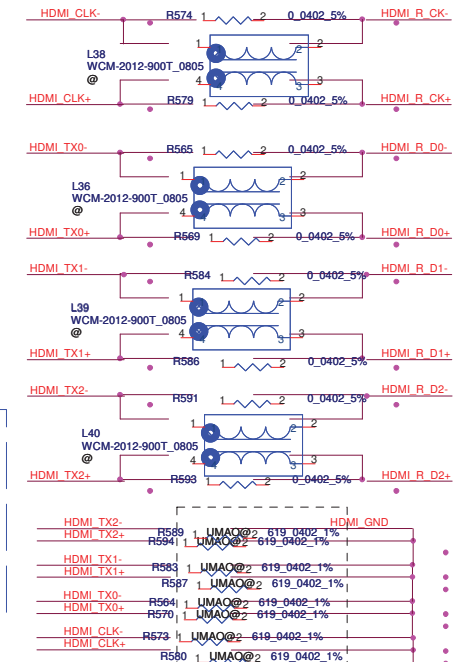
DIS



NVIDA Recommend 05/10



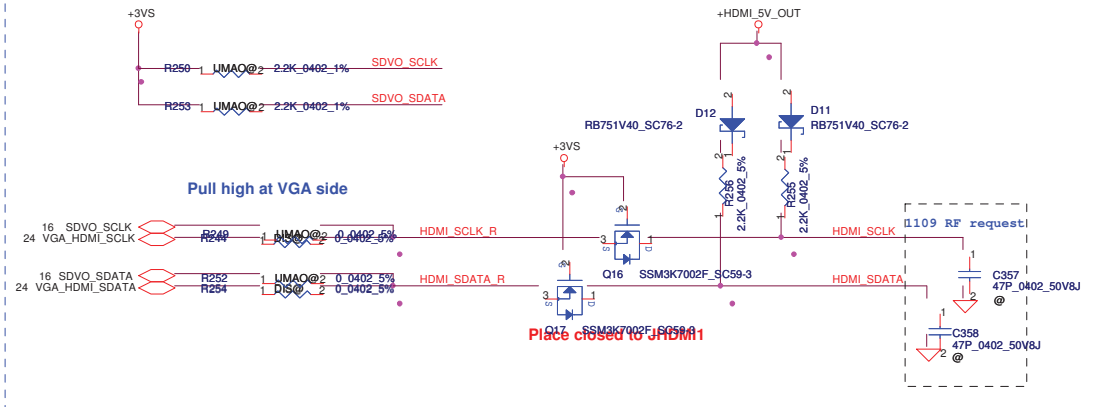
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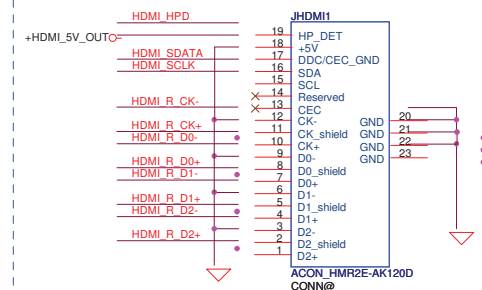
INTEL use 619 Ohm for termination

NV use 499 Ohm for termination

Pull high at VGA side



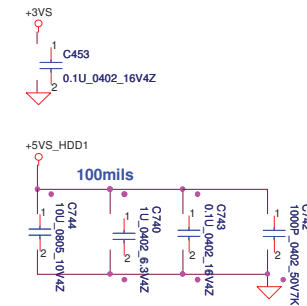
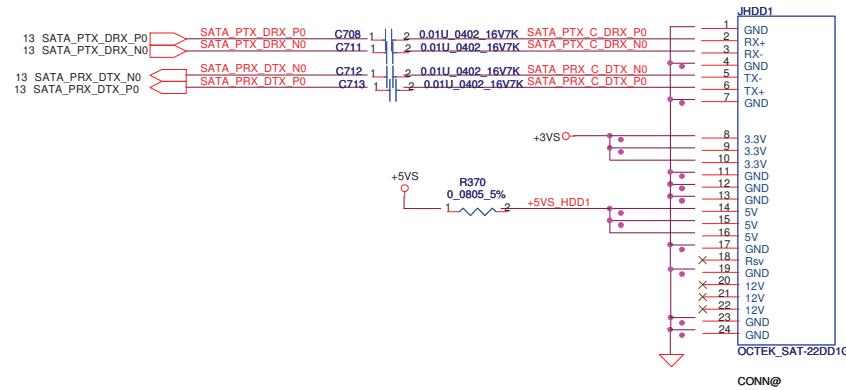
HDMI connector



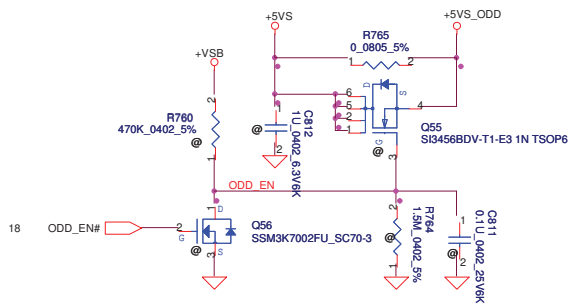
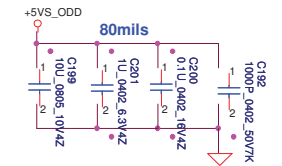
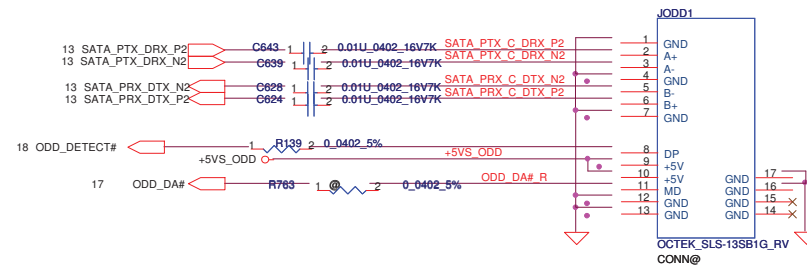
Security Classification		Compal Secret Data		Compal Electronics, Inc.						
Issued Date		2010/08/11	Deciphered Date	2011/08/11	Title	HDMI Conn				
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					Custom	P5WE0 M/B LA-6901P Schematic	0.1			
					Date:	Friday, August 27, 2010	Sheet	33	of	89

SATA HDD1 Conn.

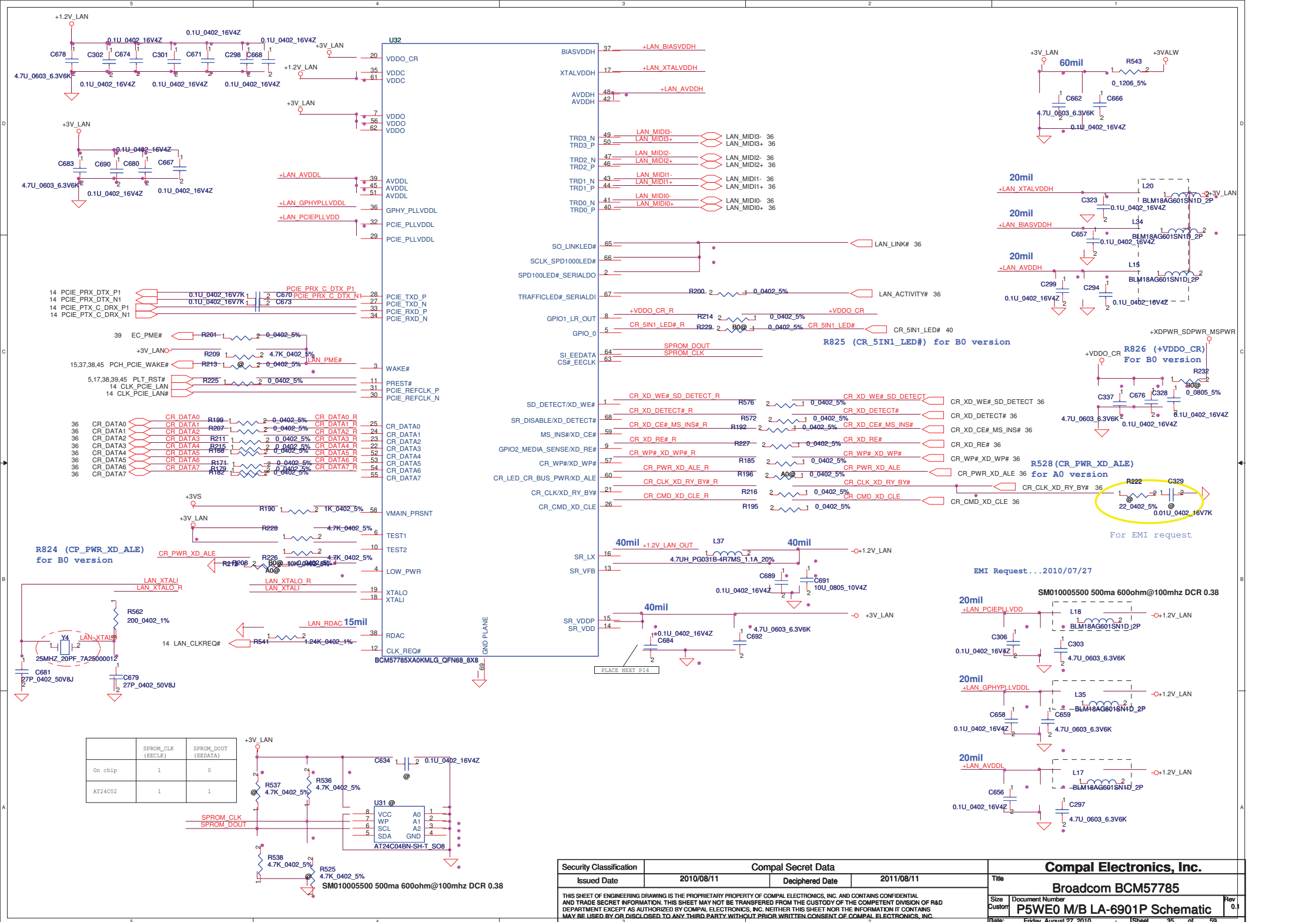
CL 4.0 mm



SATA ODD Conn.



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				Custom	P5WE0 M/B LA-6901P Schematic	0.1
				Date	Friday, August 27, 2010	Sheet 34 of 50



[illegible]

Pinout Diagram for TAITW_R013-P12-HM_NR

Left Side Connections:

- XDPWR, SDPWR, MSPWR** (Grouped): 13, 22, 43
- CR CLK XD RY BY#**: 10
- CR CMD_XD_CLE**: 19
- CR XD WE# SD_DETECT**: 1
- CR WP# XD WP#**: 2
- CR DATA0**: 4
- CR DATA1**: 3
- CR DATA2**: 25
- CR DATA3**: 23
- CR DATA4**: 21
- CR DATA5**: 17
- CR DATA6**: 8
- CR DATA7**: 5
- CR DATA0**: 12
- CR DATA1**: 14
- CR DATA2**: 18
- CR DATA3**: 20
- CR CLK XD RY BY#**: 16
- CR XD CE# MS INS#**: 9
- CR CMD_XD_CLE**: 9

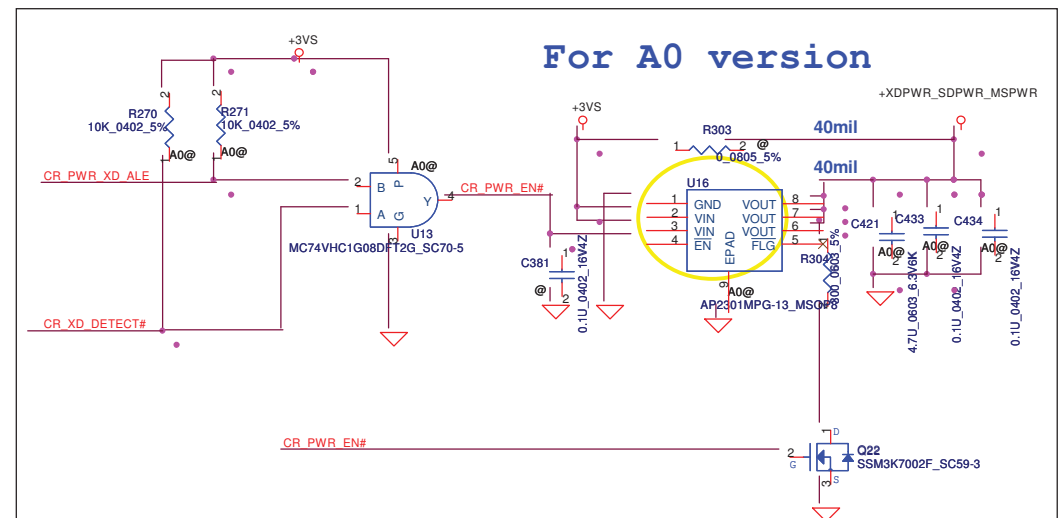
Right Side Connections:

- CR DATA0**: 35
- CR DATA1**: 36
- CR DATA2**: 37
- CR DATA3**: 38
- CR DATA4**: 39
- CR DATA5**: 40
- CR DATA6**: 41
- CR DATA7**: 42
- CR XD_DETECT#**: 26
- CR CLK XD RY BY#**: 27
- CR XD_RE#**: 28
- CR XD CE# MS INS#**: 29
- CR CMD_XD_CLE**: 30
- CR PWR XD_ALE**: 31
- CR XD WE# SD_DETECT**: 32
- CR WP# XD_WP#**: 33
- CR XD_DETECT#**: 35
- CR CLK XD RY BY#**: 35
- CR XD_RE#**: 35
- CR XD_CE# MS INS#**: 35
- CR CMD_XD_CLE**: 35
- CR PWR XD_ALE**: 35
- CR XD WE# SD_DETECT**: 35
- CR_WP#_XD_WP#**: 35

Internal Connections (JREAD1):

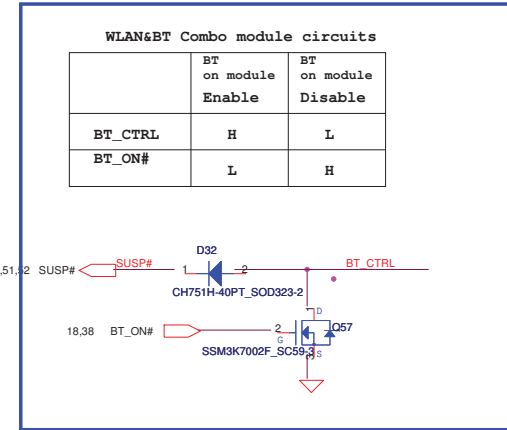
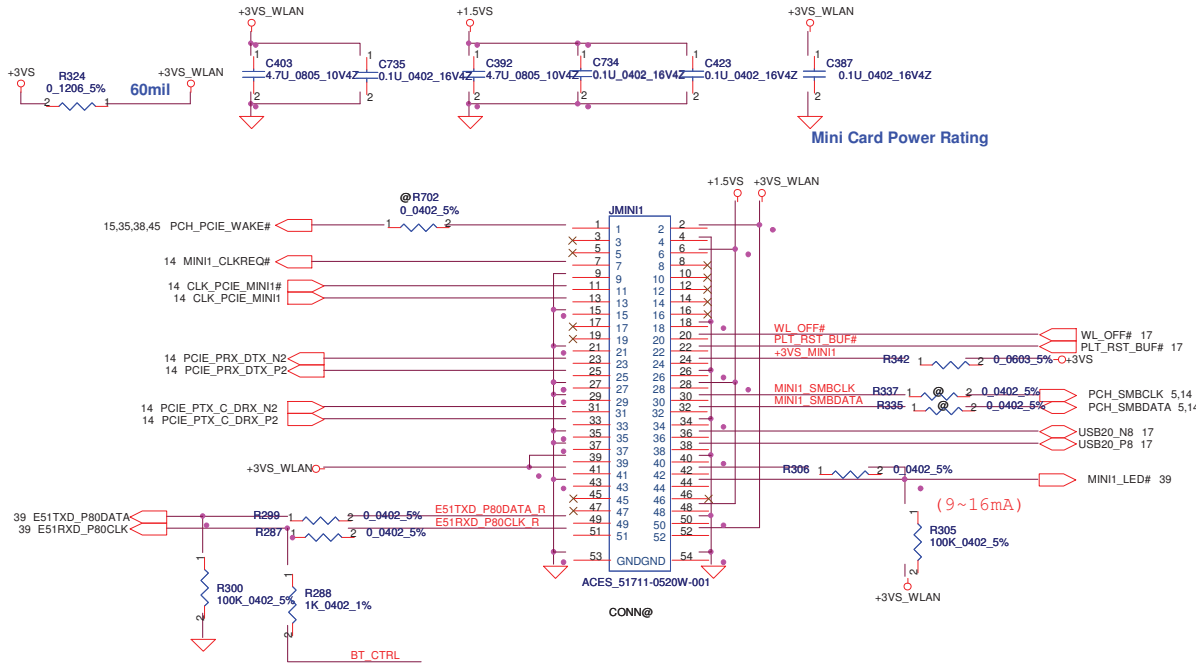
- SD_VCC**: XD_D0
- MS_VCC**: XD_D1
- XD_VCC**: XD_D2
- SD_CLK**: XD_D3
- SD_CMD**: XD_D4
- SD_CD**: XD_D5
- SD_WP**: XD_D6
- SD/MMC DAT0**: XD_CD
- SD/MMC DAT1**: XD_F/B
- SD/MMC DAT2**: XD_RE
- SD/MMC DAT3**: XD_CE
- MMC DAT4#**: XD_CLE
- MMC DAT5**: XD_ALE
- MMC DAT6**: XD_WE
- MMC DAT7**: XD_WP
- SD_GND**: 7
- SD_GND**: 15
- MS_GND**: 6
- MS_GND**: 24
- MS_GND**: 34
- XD_GND**: 44
- MS_SCLK**: 44
- MS_GND**: 45
- MS_GND**: 46

TAITW_R013-P12-HM_NR

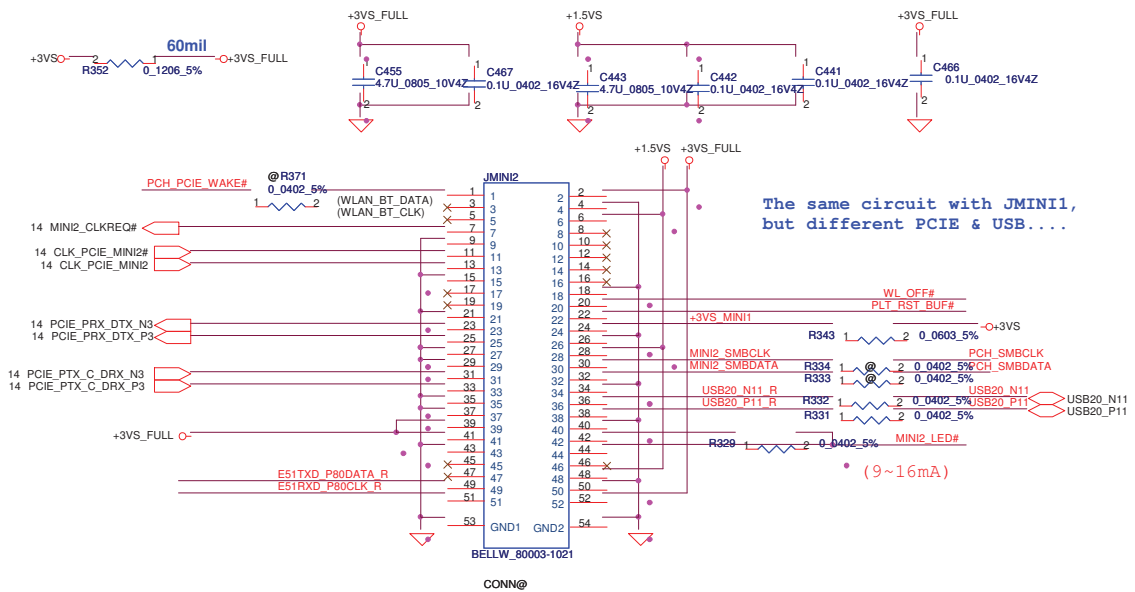


WWW.AliSaler.Com

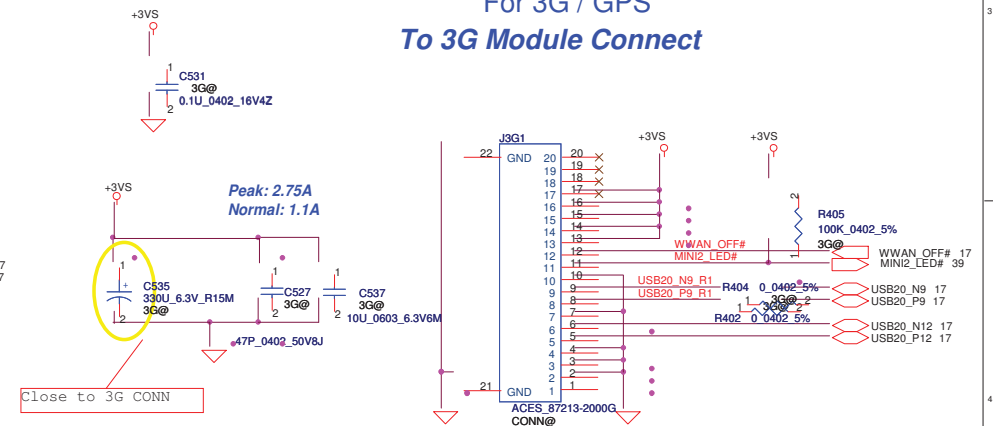
For Wireless LAN



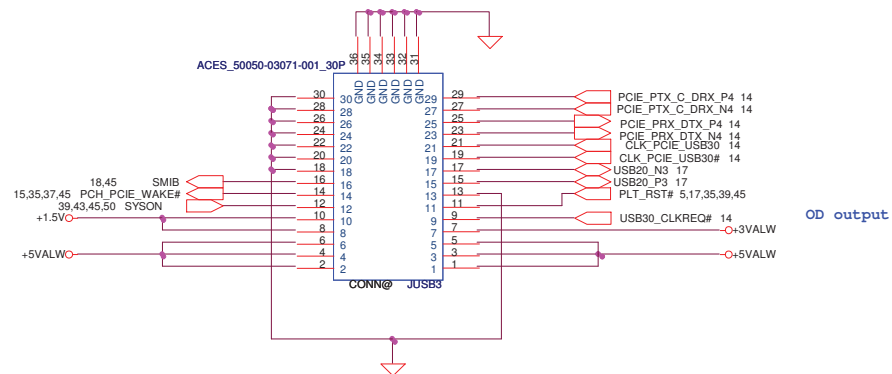
Reserve



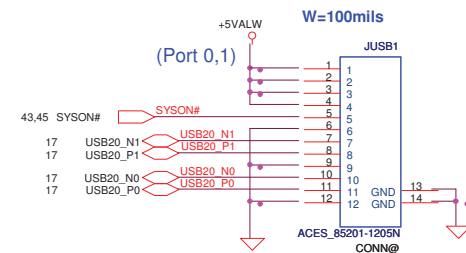
For 3G / GPS To 3G Module Connect



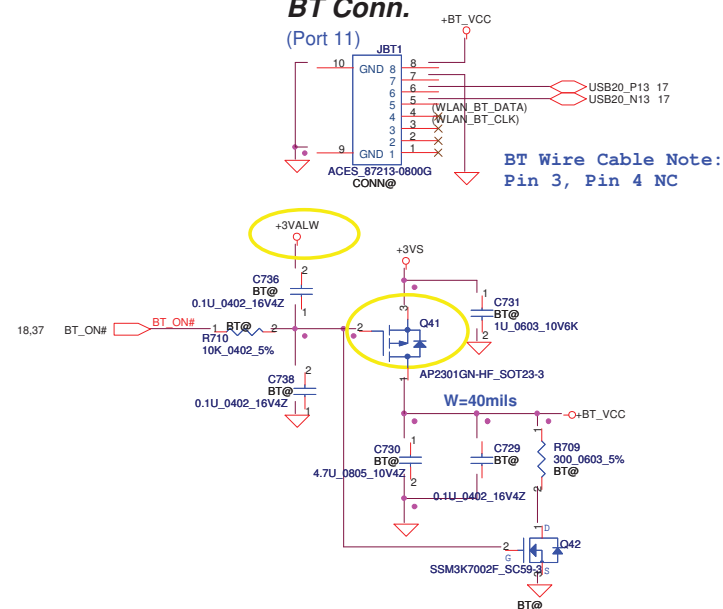
USB3.0 Conn.



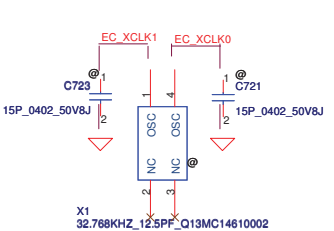
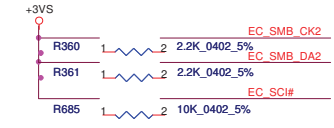
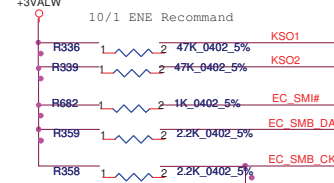
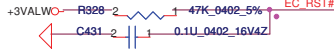
USB/B Conn.



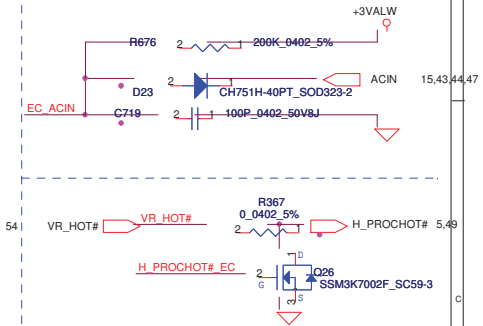
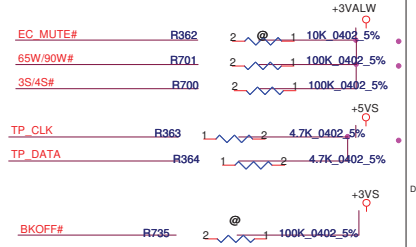
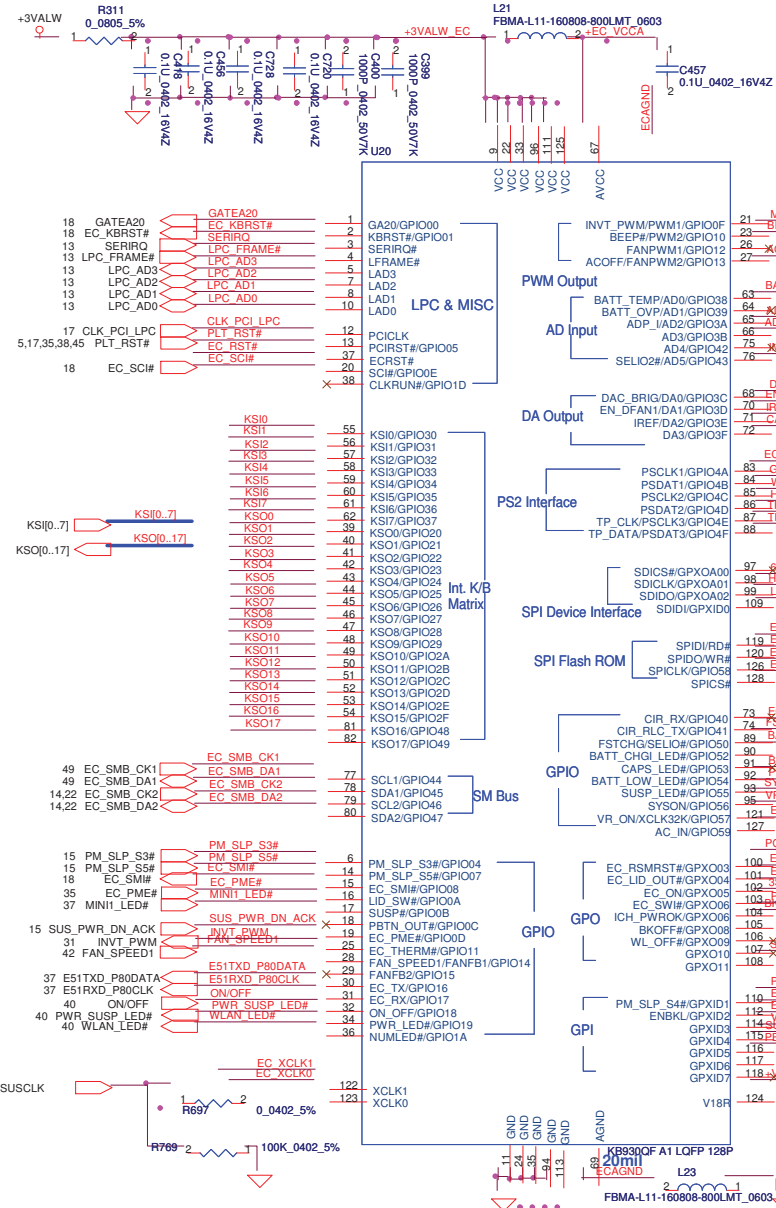
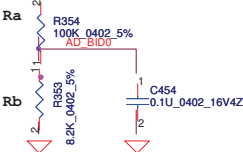
BT Conn.



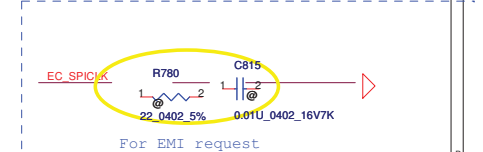
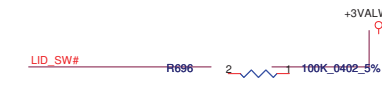
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				P5WE0 M/B LA-6901P Schematic	
				Date	Friday, August 27, 2010
				Sheet	38 of 59



Board ID
Analog Board ID definition,
Please see page 3.



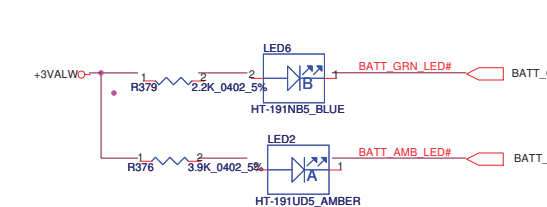
Latest design guide suggest change QE1 to 74LVC1G06.

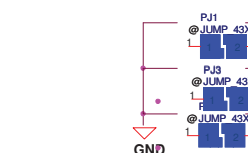
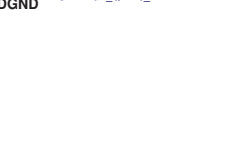
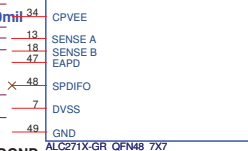
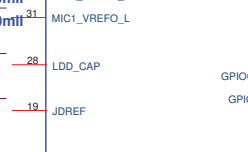
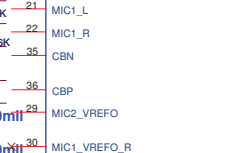
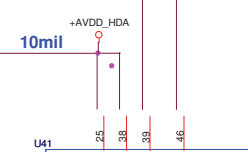
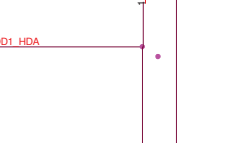
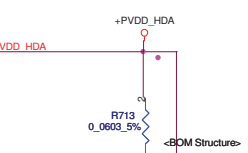
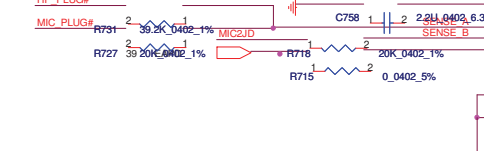
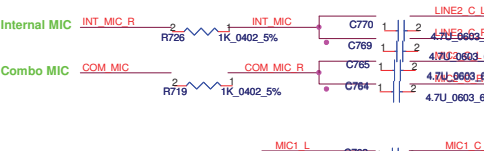
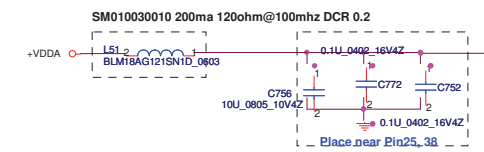
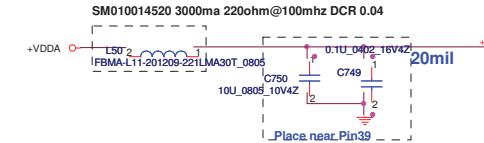
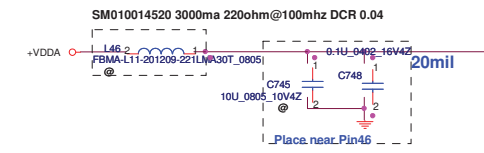
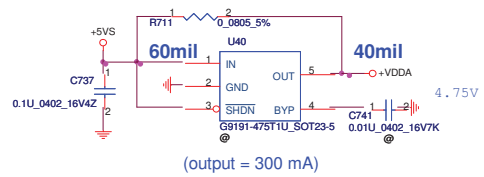


For EMI request

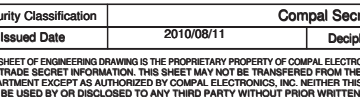
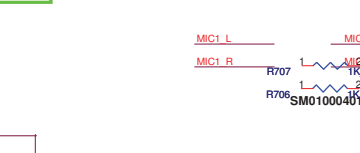
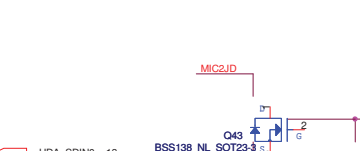
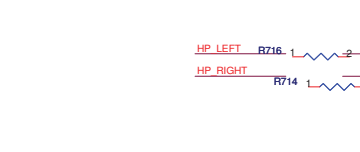
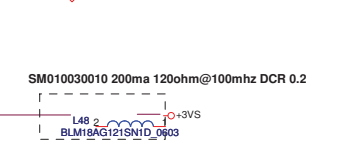
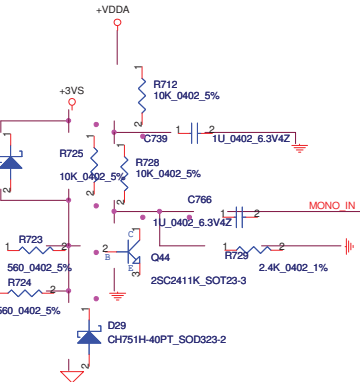
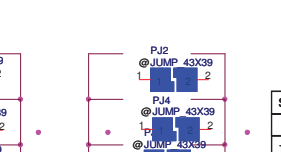
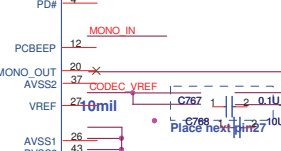
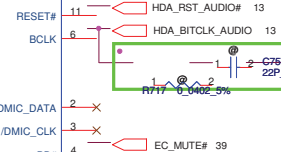
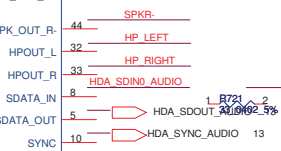
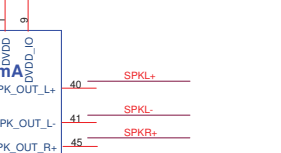
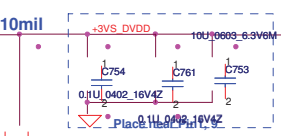


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Size	Custom	Document Number	P5WE0 M/B LA-6901P Schematic		Rev 0.1
Date	Friday, August 27, 2010	Sheet	38	of	59

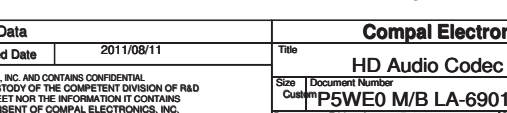
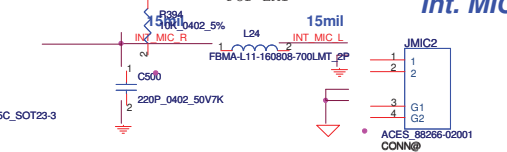
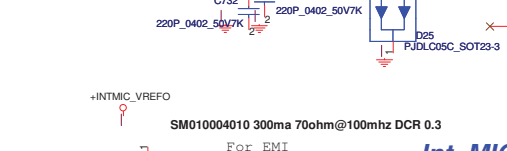
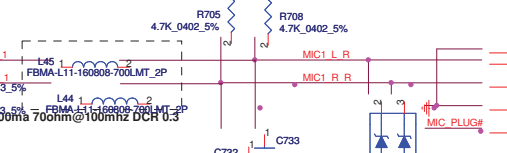
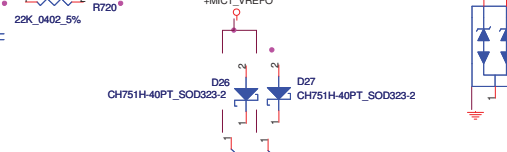
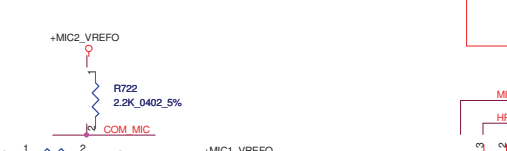
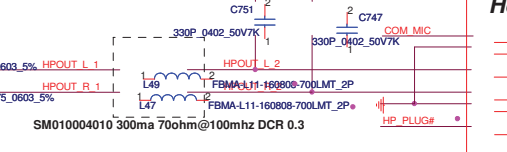
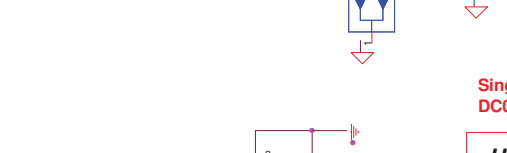
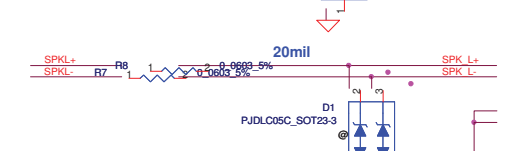
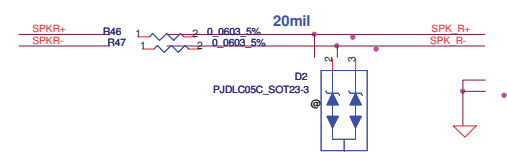




HD Audio Codec

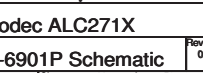
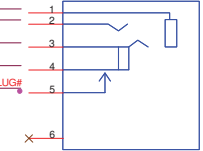
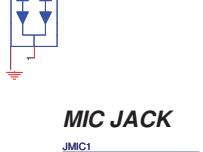
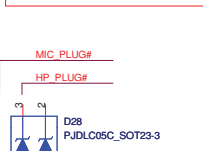
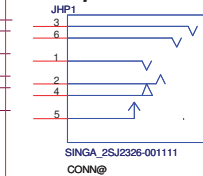


Int. Speaker Conn.

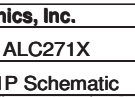
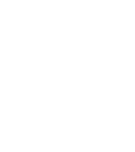
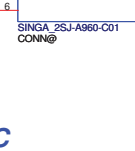
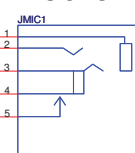


Singatron 2SJ2326 DC021007151

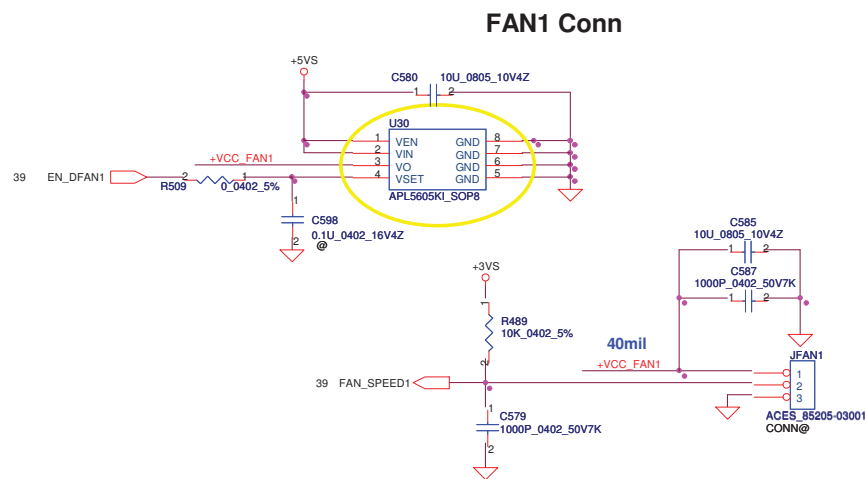
Headphone Out



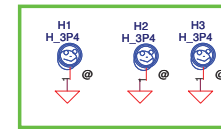
MIC JACK



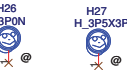
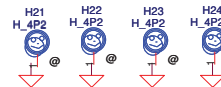
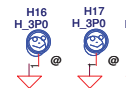
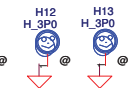
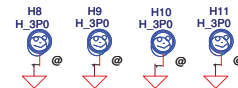
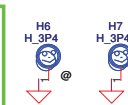
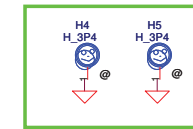
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/08/11	Deciphered Date	2011/08/11	Title	
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				Size: Document Number	
				P5WE0 M/B LA-6901P Schematic	
				Date: Friday, August 27, 2010	
				Sheet 41 of 50	



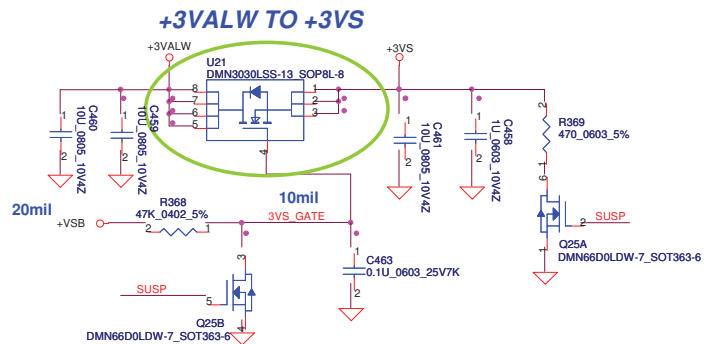
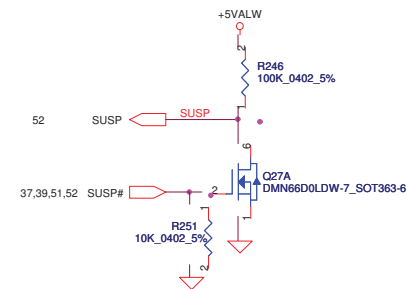
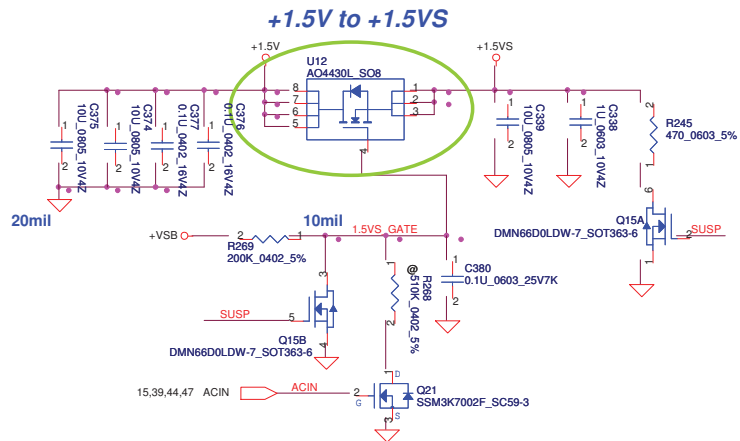
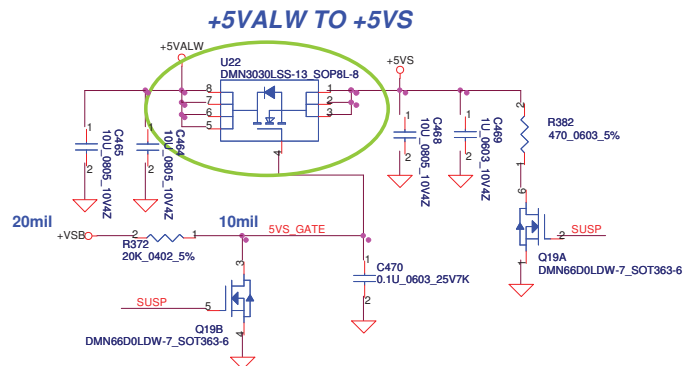
FAN Stand-Off



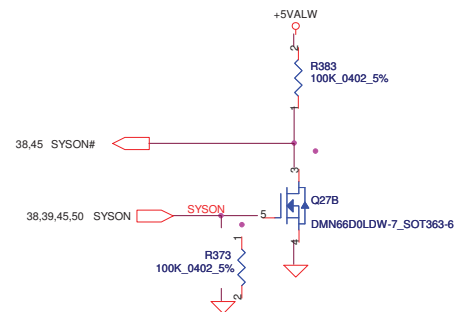
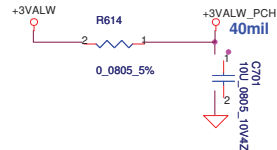
JUSB3 Stand-Off



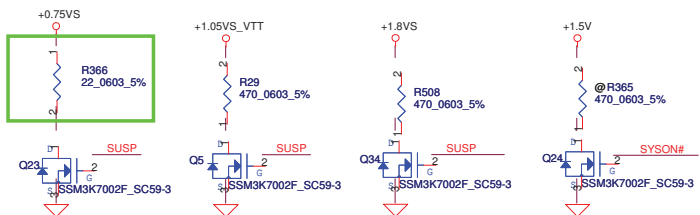
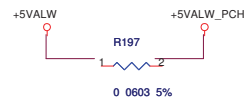
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/08/11	Deciphered Date	2011/08/11	Title	
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				Size	Document Number
				Custom	P5WE0 M/B LA-6901P Schematic
				Date:	Friday, August 27, 2010
				Sheet	42 of 59
				Rev	0.1



+3VALW TO +3VALW_PCH(PCH AUX Power)

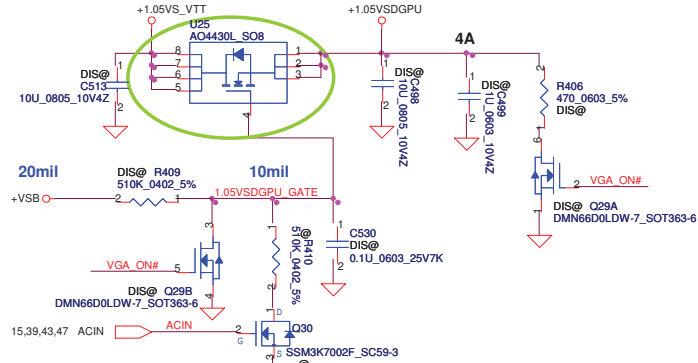


+5VALW TO +5VALW_PCH(PCH AUX Power)

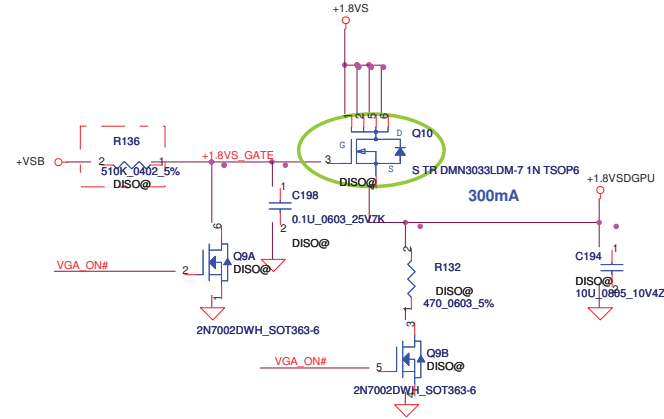


Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2010/08/11	Deciphered Date	2011/08/11	Title	DC Interface	
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				Customer	P5WE0 M/B LA-6901P Schematic	
				Date: Friday, August 27, 2010		Sheet 43 of 50

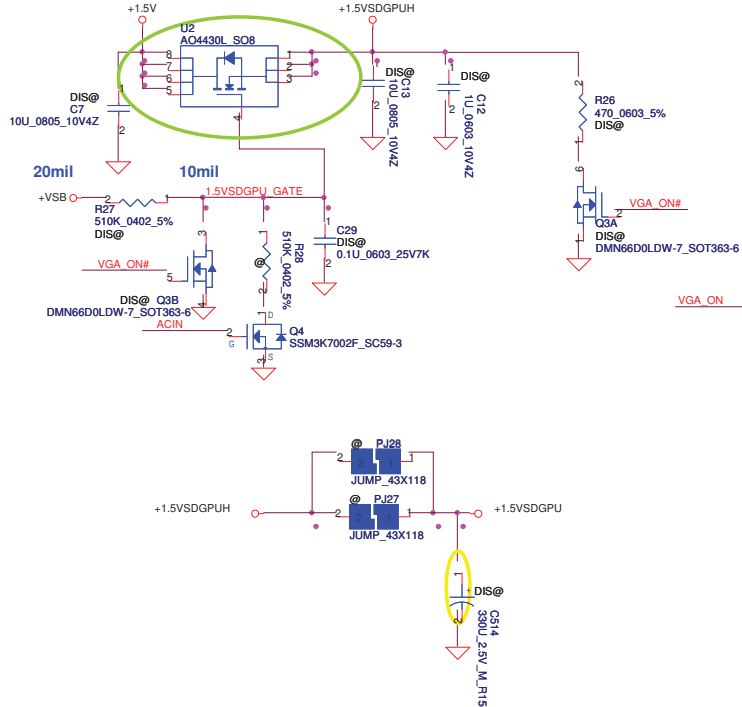
+1.05VS_VTT to +1.05VSDGPU for GPU



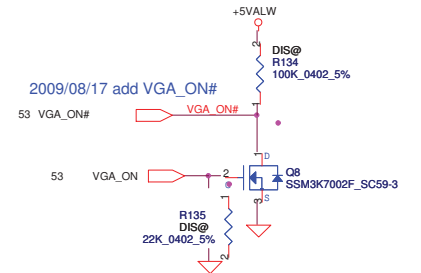
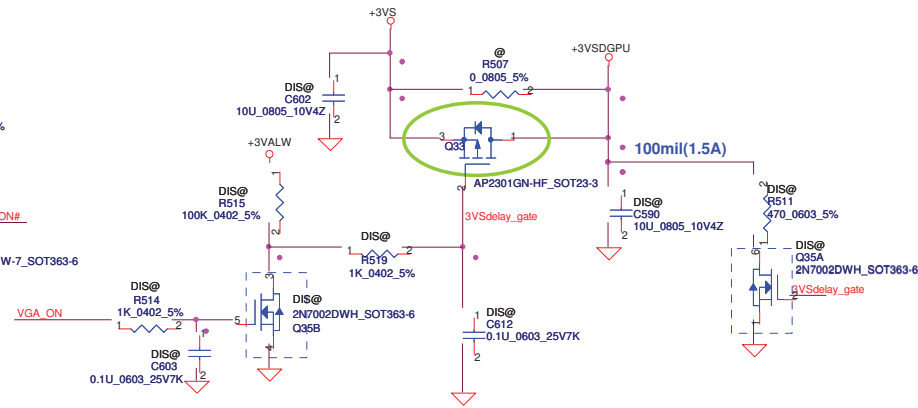
+1.8VS to +1.8VSDGPU for GPU



+1.5V to +1.5VSDGPUH for GPU

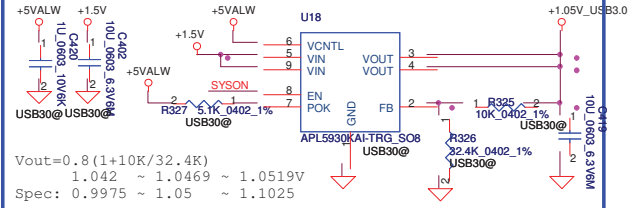


+3VS to +3VSDGPU for GPU

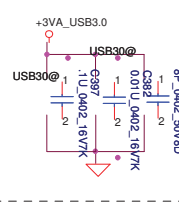


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				DC Interface	
Size		Document Number		Rev	
P5WE0		M/B LA-6901P Schematic		0.1	
Date:		Friday, August 27, 2010		Sheet 44 of 50	

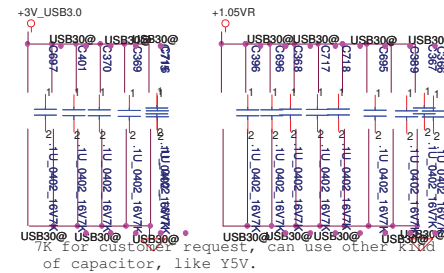
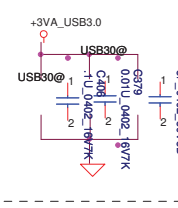
+1.5V to +1.05V Transfer



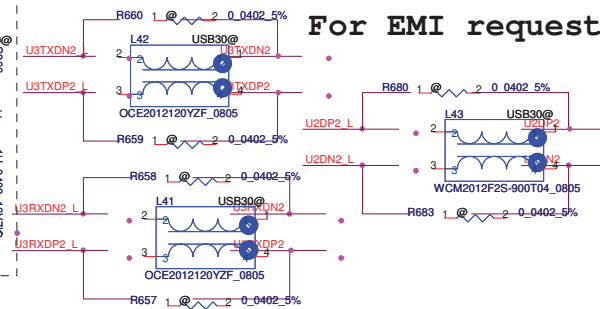
Close to U3.D7



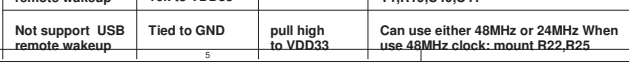
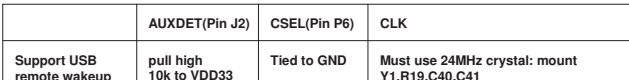
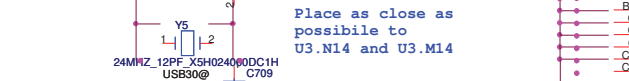
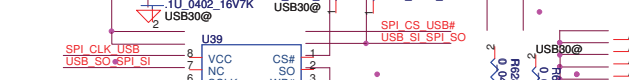
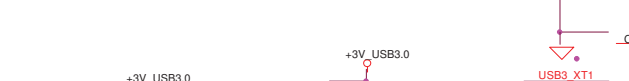
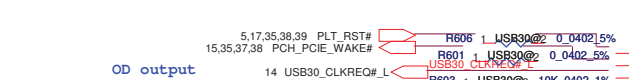
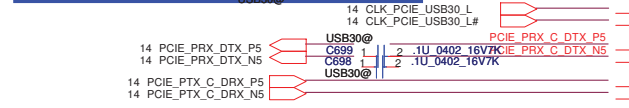
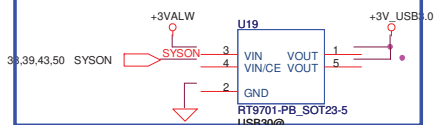
Close to U3.P13



For EMI request



+3VALW to +3V Transfer

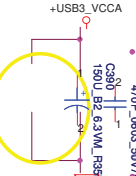


SPEC Max: +3V---200mA; +1.05V---800mA
Idle mode: 0.489W;
+3V---43mA; +1.05V---328mA
D3 mode: 0.066W;
+3V---5.4mA; +1.05V---45mA

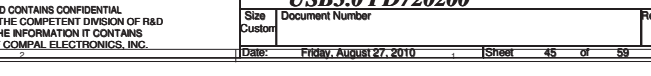
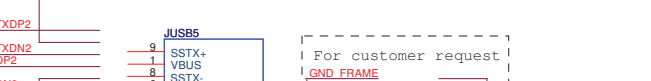
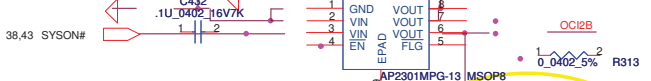
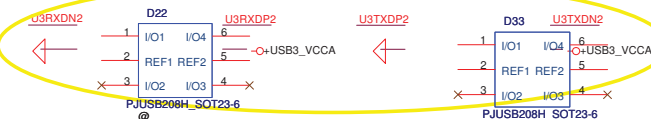
Can be attach to EC, either.

PCI Express/ExpressCard select signal
 1: others
 0: Express Card or Mini card

As short as possible



For ESD request

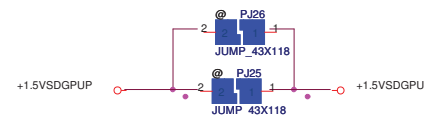
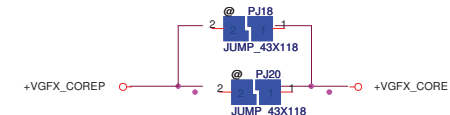
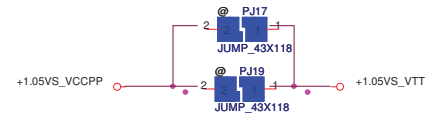
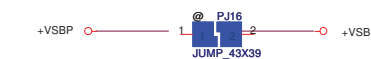
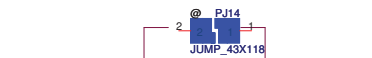
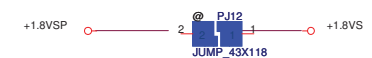
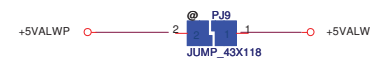
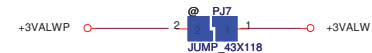
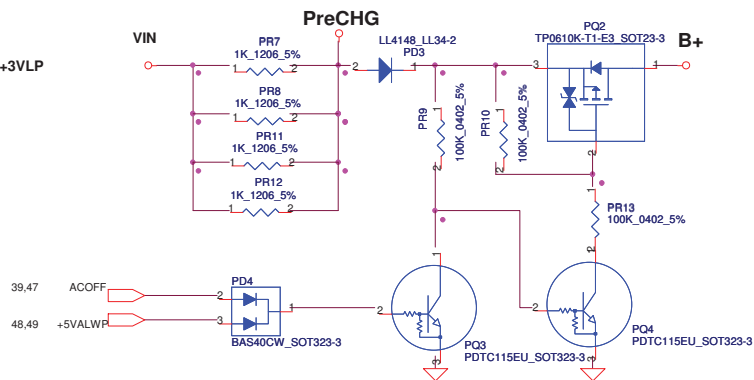
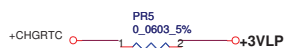
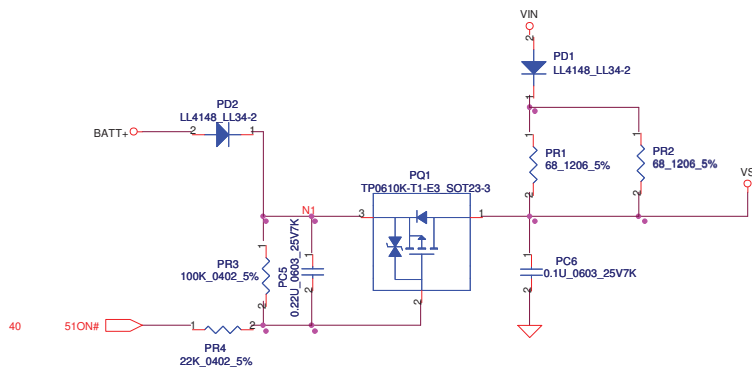
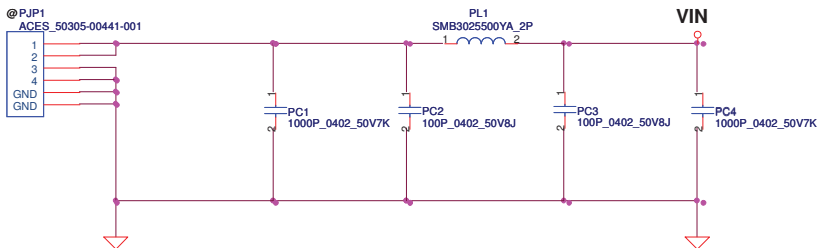


Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

UPD72020AF1-DAP-A FBGA176-USB30@

Security Classification		Compal Secret Data		Title USB3.0 PD720200	
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				Date: Friday, August 27, 2010	Sheet 45 of 59



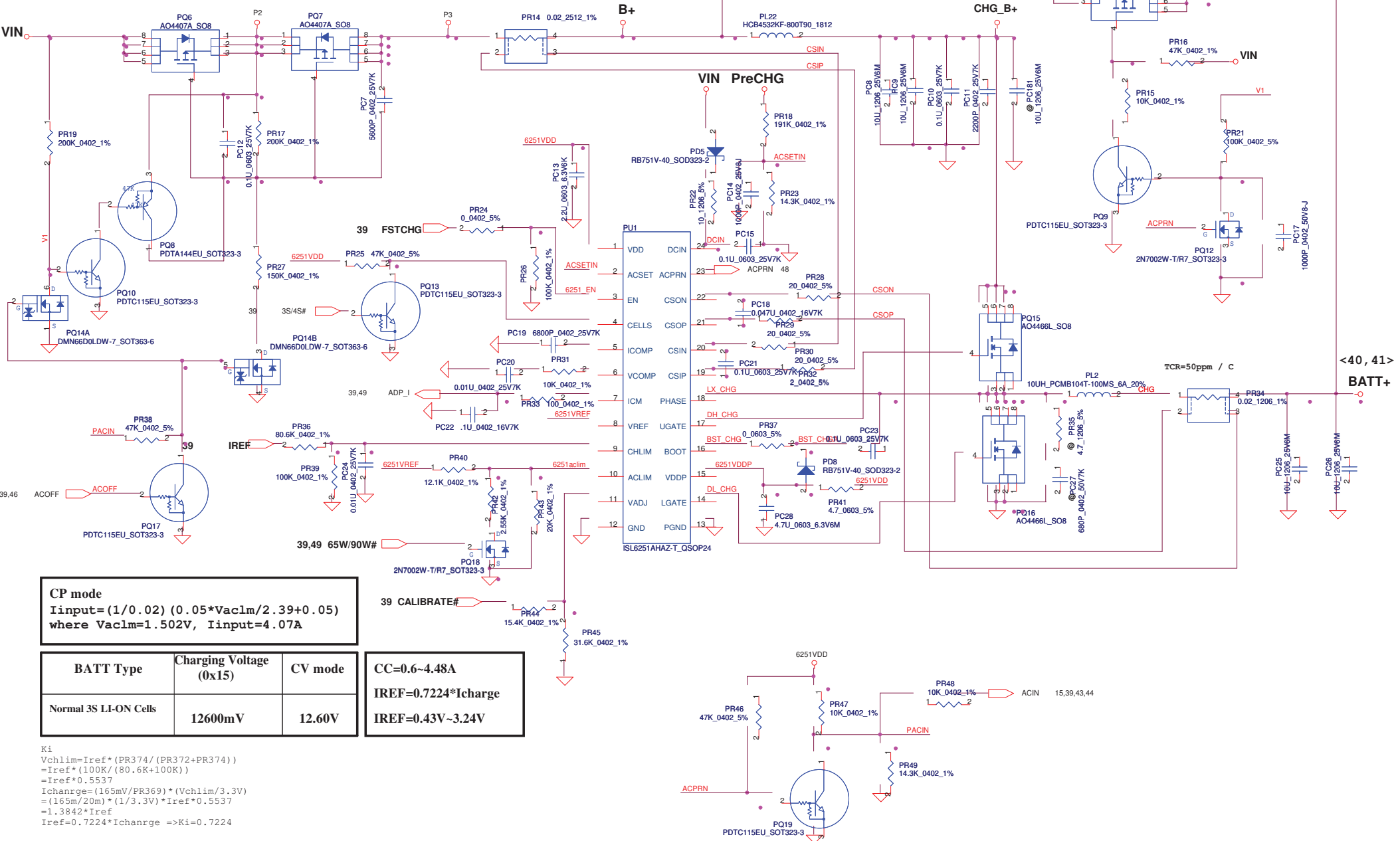
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2010/07/13	Deciphered Date	2011/07/13	Title	PWR DCIN / Pre-charge	
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				Custom	P5WE0 M/B LA-6901P Schematic	0.1
				Date	Friday, August 27, 2010	Sheet 46 of 59

Iada=0~4.74A (90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A

PC181 reserve for EMI Isen solution



CP mode

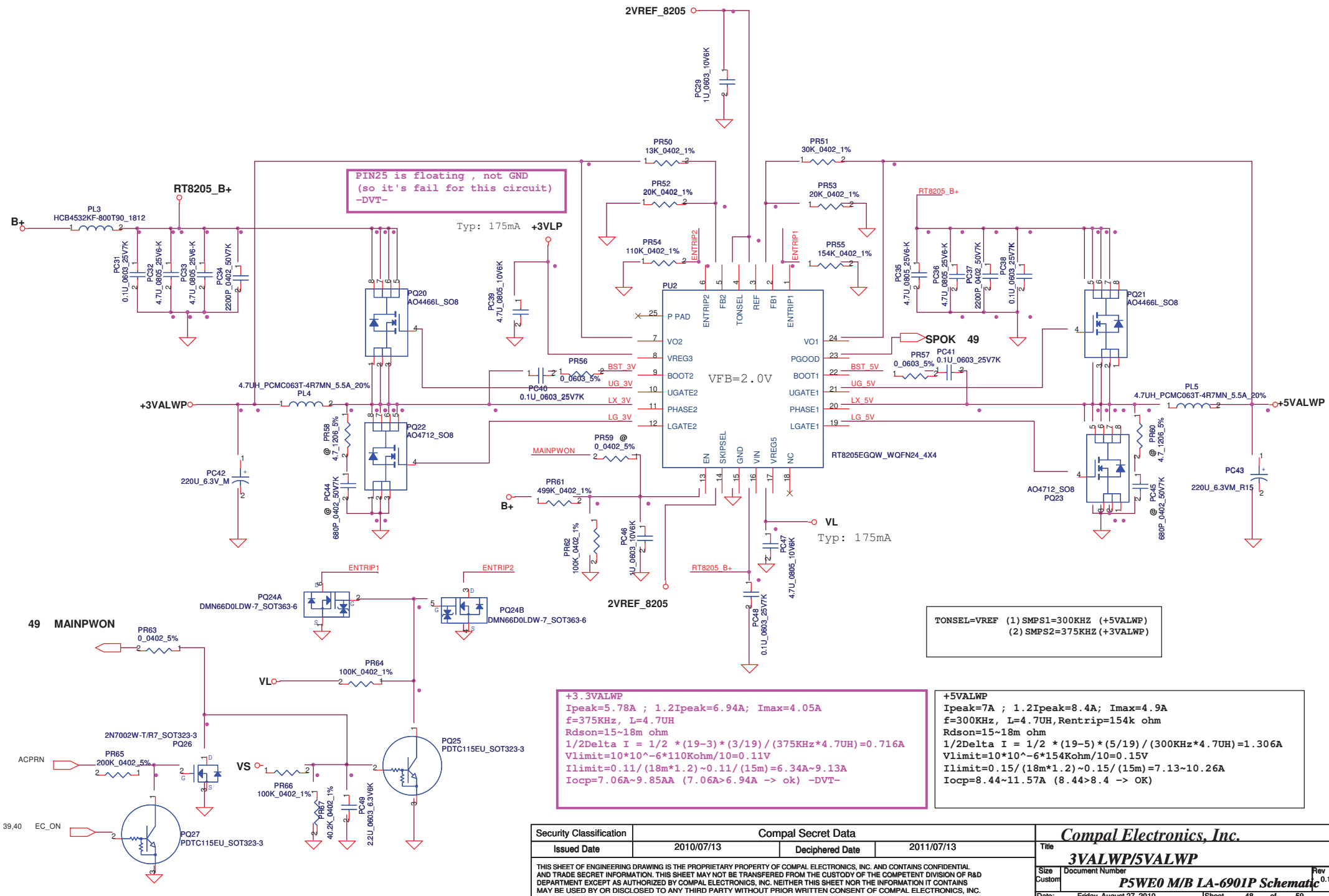
$I_{input} = (1/0.02) (0.05 \cdot V_{ac1m} / 2.39 + 0.05)$
where $V_{ac1m} = 1.502V$, $I_{input} = 4.07A$

BATT Type	Charging Voltage (0x15)	CV mode	CC=0.6~4.48A IREF=0.7224*Icharge IREF=0.43V~3.24V
Normal 3S LI-ON Cells	12600mV	12.60V	

Ki
 $V_{chlim} = I_{ref} * (PR374 / (PR372 + PR374))$
 $= I_{ref} * (100K / (80.6K + 100K))$
 $= I_{ref} * 0.5537$
 $I_{charge} = (165mV / PR369) * (V_{chlim} / 3.3V)$
 $= (165m / 20m) * (1/3.3V) * I_{ref} * 0.5537$
 $= 1.3842 * I_{ref}$
 $I_{ref} = 0.7224 * I_{charge} \Rightarrow Ki = 0.7224$

Kv
 $R_{internal} = 514K$ $R_{ec} = 3K$ $R_1 = PR379 = 15.4K$ $R_2 = PR381 = 31.6K$
 $R = 514K / (31.6K / ((15.4K + 3K) * 11.372K))$
 $r = 514K / (514K / (31.6K * 28.14K))$
 $V_{cell} = 0.175 * V_{adj} + 3.99V$
 $4.2V = 0.175 * V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$
 $V_{adj} = V_{ref} * (R / (R + 514K)) + CALIBRATE * (r / (r + 514K))$
 $1.1483 = CALIBRATE * 0.6046 \Rightarrow CALIBRATE = 1.899$
 $1.899 = (4.2 - (V_{cell} + A * 0.175)) * Kv = (4.2 - (4.2 + A * 0.175)) * Kv$
 $A = V_{ref} * (R / (R + 514K)) = 0.052$
 $Kv = 9.451$

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Issued Date	2010/07/13	Deciphered Date	2011/07/13	Title	PWR-CHARGER
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				Custom	PSWE0 M/B LA-6901P Schematic
				Date	Friday, August 27, 2010
				Sheet	47 of 58
				Rev	0.1



PIN25 is floating , not GND
(so it's fail for this circuit)
-DVT-

Typ: 175mA +3VLP

VFB=2.0V

Typ: 175mA

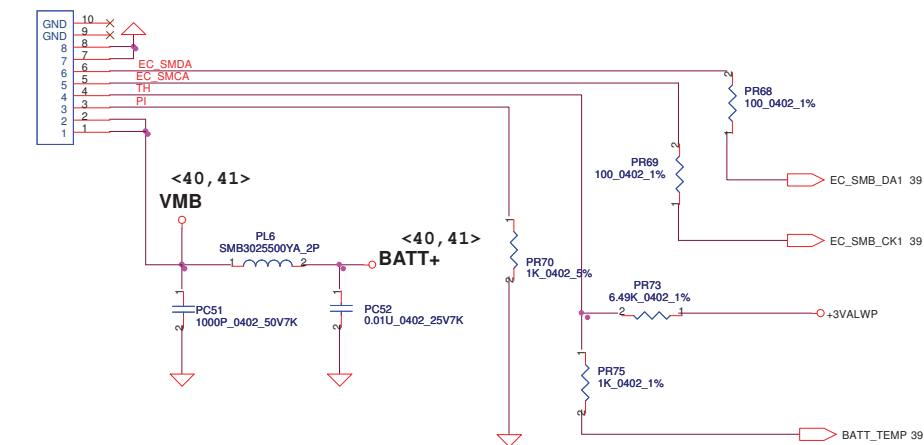
TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
(2) SMPS2=375KHZ (+3VALWP)

+3.3VALWP
Ipeak=5.78A ; 1.2Ipeak=6.94A; Imax=4.05A
f=375KHz, L=4.7UH
Rdson=15~18m ohm
 $1/2\Delta I = 1/2 * (19-3) * (3/19) / (375KHz * 4.7UH) = 0.716A$
Vlimit=10*10^-6*110Kohm/10=0.11V
Ilimit=0.11/(18m*1.2)~0.11/(15m)=6.34A~9.13A
Iocp=7.06A~9.85AA (7.06A>6.94A -> ok) -DVT-

+5VALWP
Ipeak=7A ; 1.2Ipeak=8.4A; Imax=4.9A
f=300KHz, L=4.7UH, Rentrip=154k ohm
Rdson=15~18m ohm
 $1/2\Delta I = 1/2 * (19-5) * (5/19) / (300KHz * 4.7UH) = 1.306A$
Vlimit=10*10^-6*154Kohm/10=0.15V
Ilimit=0.15/(18m*1.2)~0.15/(15m)=7.13~10.26A
Iocp=8.44~11.57A (8.44>8.4 -> OK)

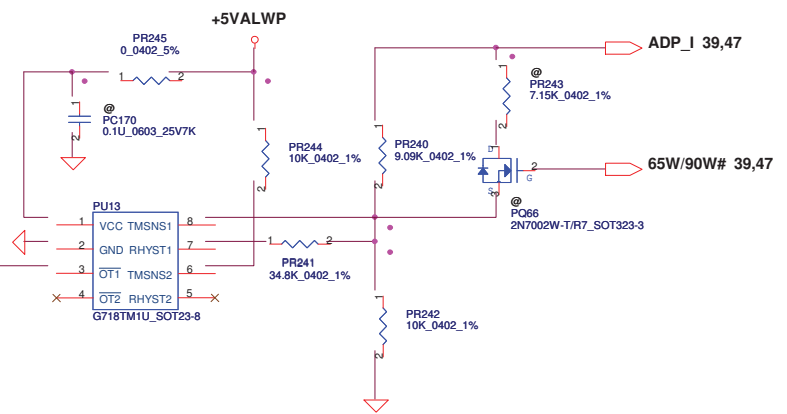
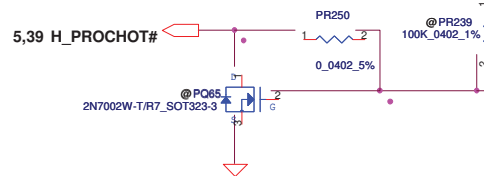
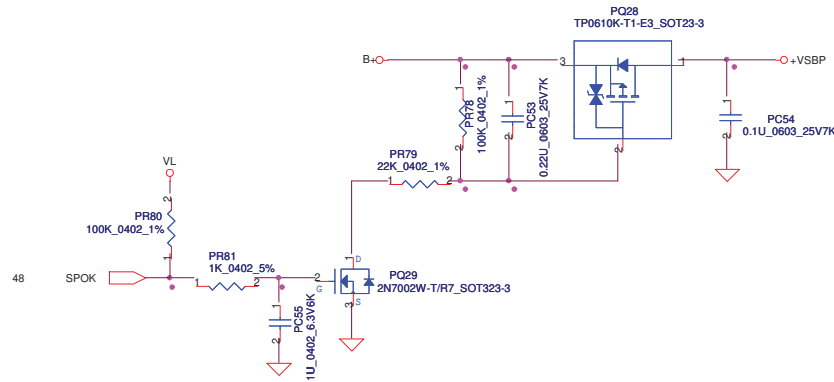
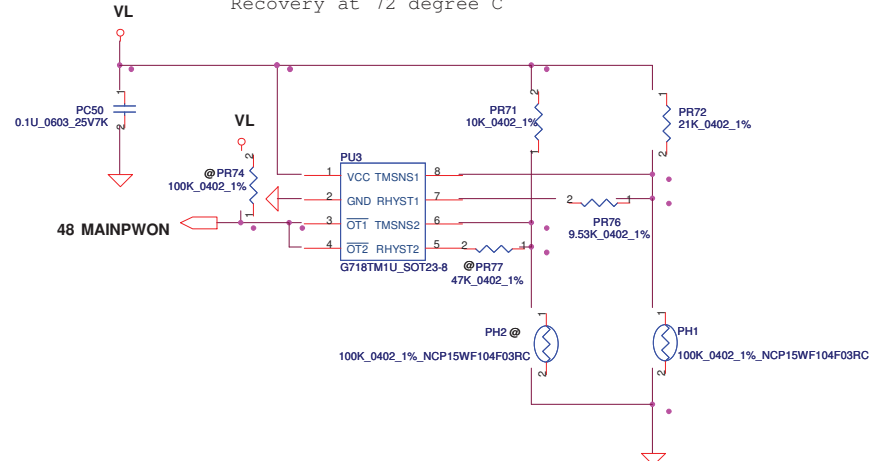
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				Size	Document Number	Rev
				Custom	P5WE0 M/B LA-6901P Schematic	0.1
Date:	Friday, August 27, 2010	Sheet	48	of	59	

PJP2
SUYIN_200275GR008G13GZR

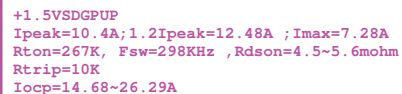
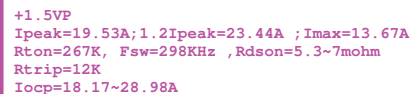


PH1 under CPU botten side :

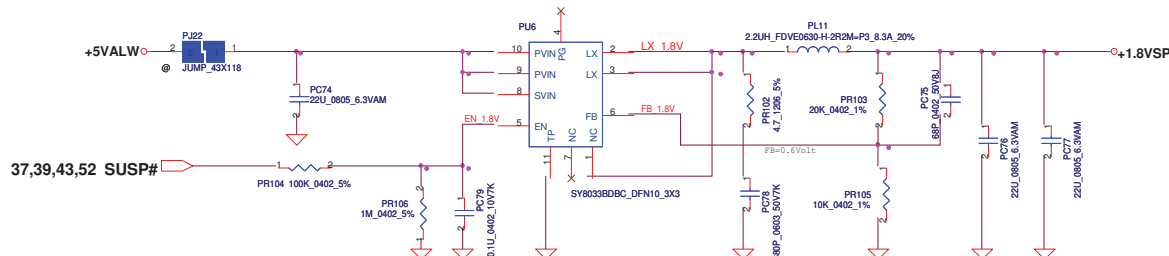
CPU thermal protection at 92 degree C
Recovery at 72 degree C



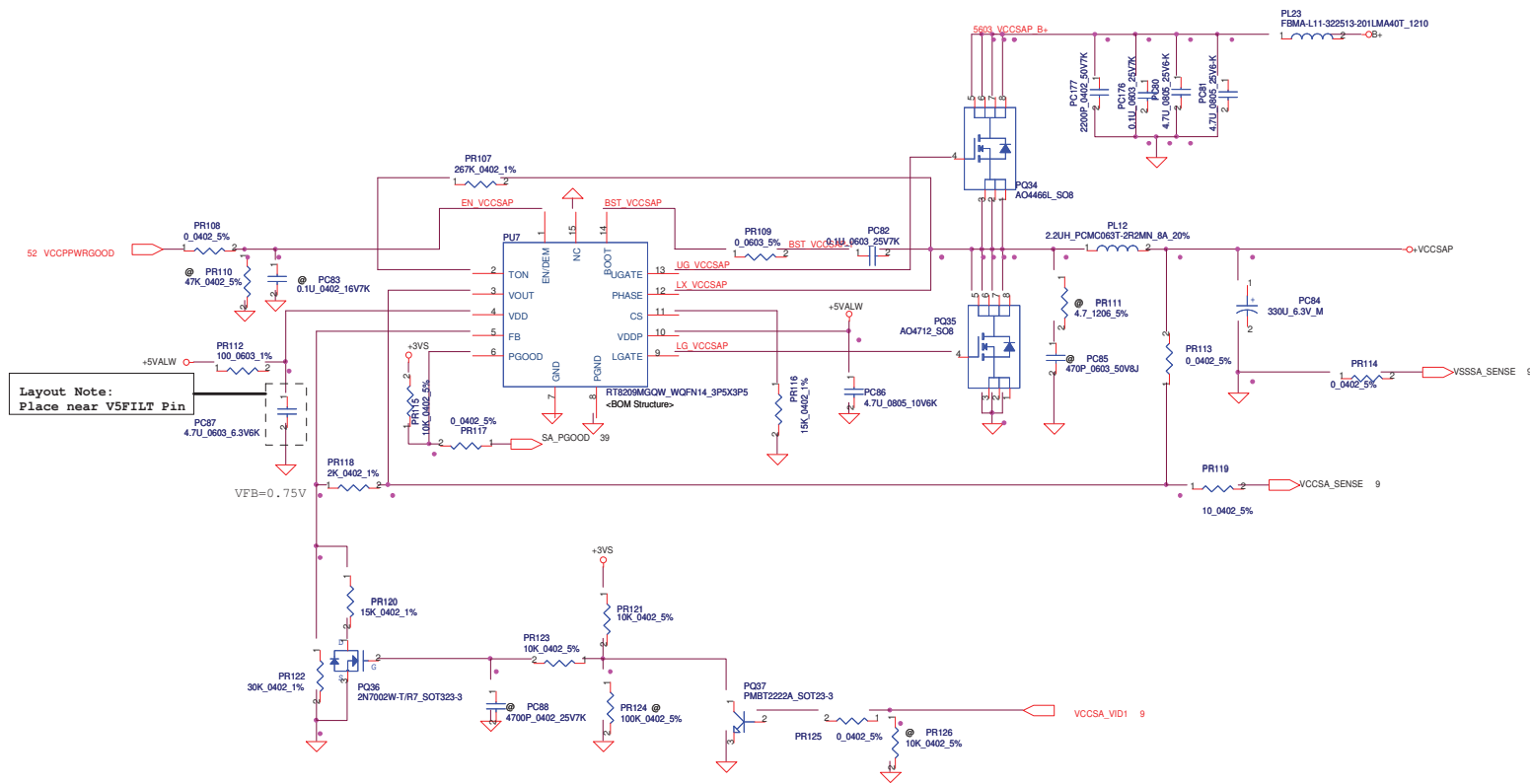
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				Size	Document Number	Rev
				Custom	P5WE0 M/B LA-6901P Schematic	0.1
				Date	Friday, August 27, 2010	Sheet 49 of 59



Security Classification		Compal Secret Data		Compal Electronics, Inc. PWR-+1.5VP/+1.5VSDGPU	
Issued Date	2010/07/13	Deciphered Date	2011/07/13	Title	
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				Document Number	0.1
				P5WE0 M/B LA-6901P Schematic	
Date:	Friday, August 27, 2010	1 Sheet	50 of 50		



1.8VSP
 $I_{peak}=3.35A$; $1.2I_{peak}=4.02$; $I_{max}=2.345A$
 $V_{out}=0.6 \cdot (1 + (20K/10K)) = 1.8V$
 -DVT-



Layout Note:
 Place near V5FILT Pin

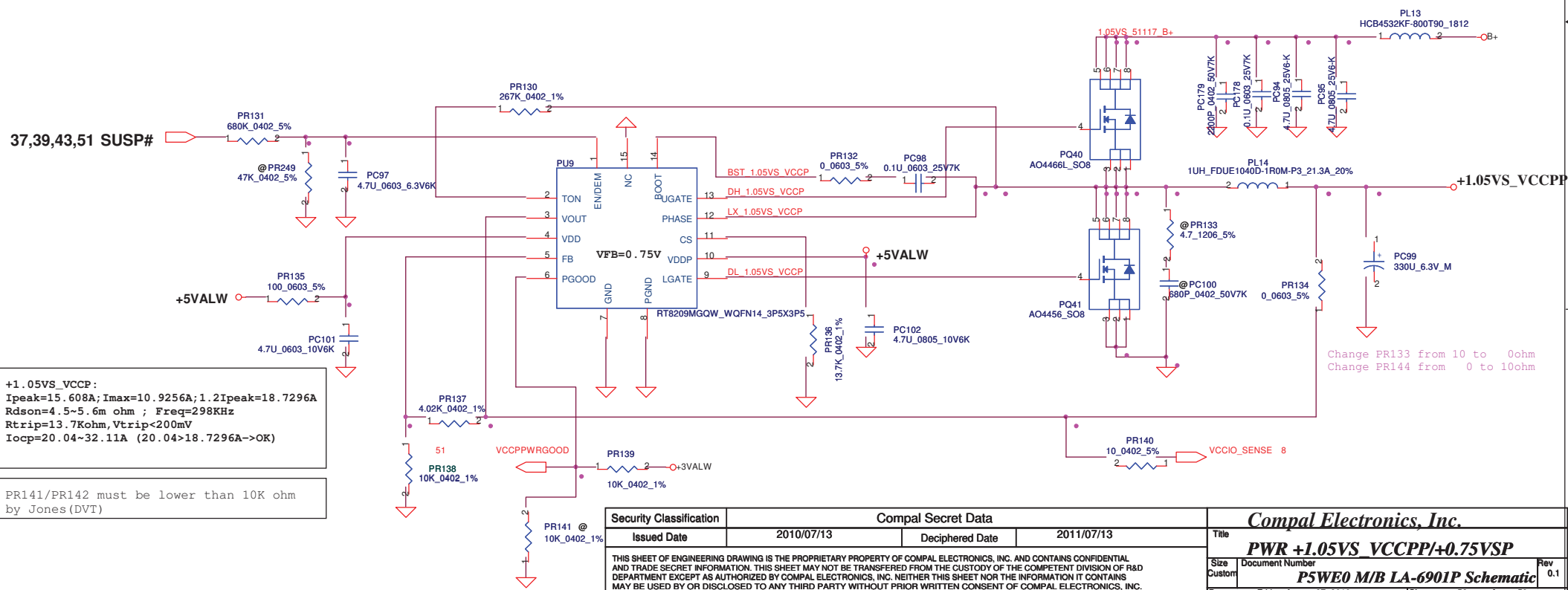
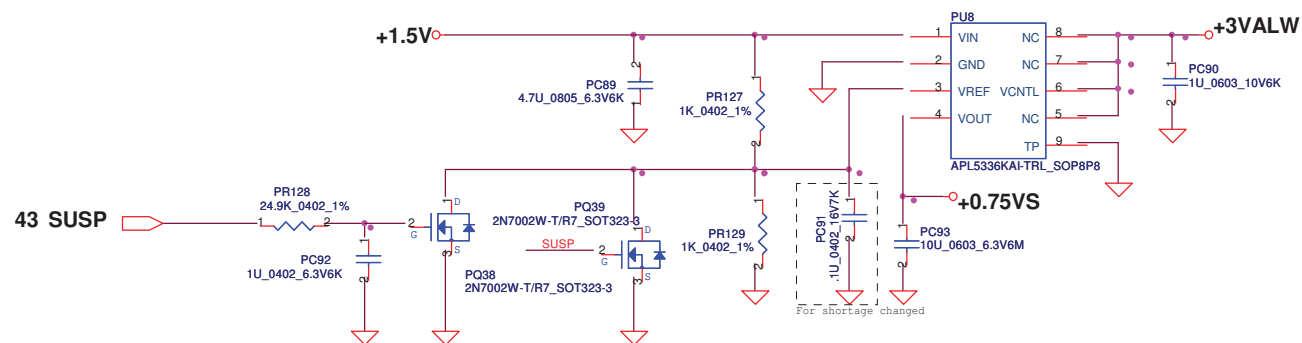
$V_{FB}=0.75V$
 $V_o = V_{FB} \cdot (1 + PR156/PR150) = 1.1V$
 $T_{on} = 19E-12 \cdot Ron \cdot ((2/3) \cdot V_o + 150mV) / V_{in} + 50ns = 2.4E-7$
 $Freq = 282KHz$
 $C_{esr} = 15m \text{ ohm}$
 $I_{peak} = 4.60A$ $I_{max} = 2.70A$
 $\Delta I = ((19.5 - 1.0) \cdot (1.0/19.5)) / (L \cdot Freq) = 1.48A$
 $V_{trip} = R_{trip} \cdot I_{peak} = 0.0787V$
 $I_{ocp_min} = 5.96A$
 $I_{ocp_max} = 6.01A$
 $I_{ocp} = 5.96 - 6.01A$

VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012	Required
0	0	0.9 V	Yes/Yes	
0	1	0.8 V	Yes/Yes	
1	1	0.75V	No/Yes	
1	1	0.65V	No/Yes	

Note: Use VCCSA_SEL to switch High & Low Level for VID[1]
 (ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

+VCCSA
 $I_{peak}=6A$, $I_{max}=4.2A$, $1.2I_{peak}=7.2A$
 $DCR = 9 \text{ m} (typ) \sim 10 \text{ m} (max)$
 $R_{limit}=12K$, $R_{dson}=15-18mohm$
 $I_{limit}=10uA$
 $I_{ocp}=R_{limit}/R_{dson} \cdot 10^{-5} = 7.59 - 10.654A$

the resister change
 from @ to pop component
 Add two jumpers on the HW's output cap of the
 +VCCSA's PIN(+) and PIN(-) to sense the
 feedback voltage for VCCSA_SENSE & VSSSA_SENSE.

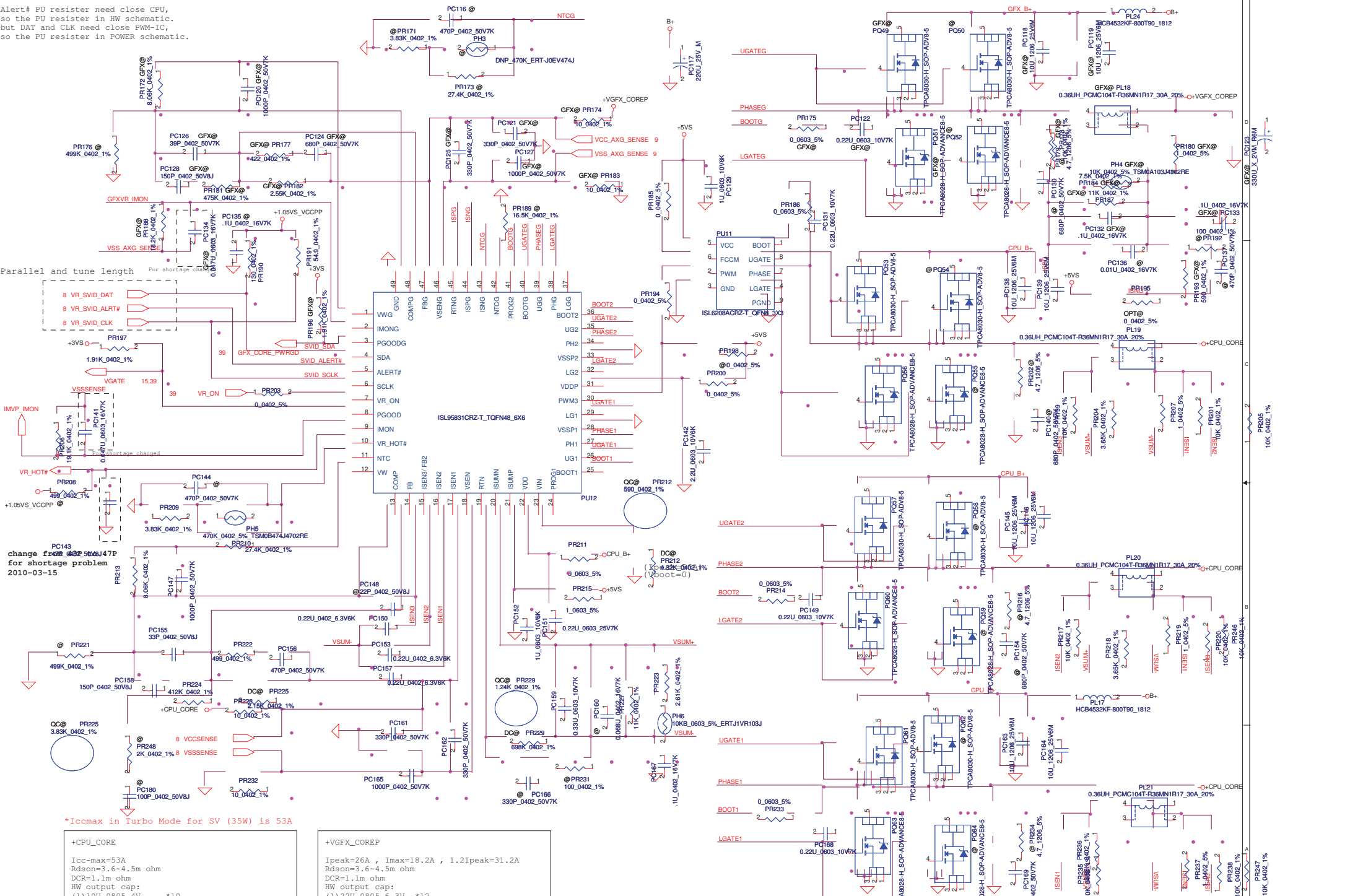


+1.05VS_VCCPP:
 Ipeak=15.608A; Imax=10.9256A; 1.2Ipeak=18.7296A
 Rdson=4.5~5.6m ohm ; Freq=298KHz
 Rtrip=13.7Kohm, Vtrip<200mV
 Iocp=20.04~32.11A (20.04>18.7296A->OK)

PR141/PR142 must be lower than 10K ohm
 by Jones (DVT)

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				Document Number	P5WE0 M/B LA-6901P Schematic
				Date:	Friday, August 27, 2010
				Sheet	52 of 59

Alert# PU resistor need close CPU,
so the PU resistor in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resistor in POWER schematic.



Parallel and tune length

change for 5VCC for shortage problem
2010-03-15

*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE

Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1) 100U_0805_4V *10
(2) 22U_0805_6.3V *15
(3) 470U_D2_2V *4 (ESR=4.5m ohm)

*OCP setting value=71.5A

+VGFX_COREP

Ipeak=26A, Imax=18.2A, 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1) 22U_0805_6.3V *12
(2) 470U_D2_2V *2 (ESR=4.5m ohm)

*OCP setting value=37A

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Size		PWR +CPU CORE/+VGFX CORE	
Customer		P5WE0 M/B LA-6901P Schematic	
Date		Friday, August 27, 2010	
Sheet		54 of 58	

5

4

3

2

1

Page 1 of 1

Version change list (P.I.R. List) for PWR

Item	Fixed Issue	Reason for change	Rev	PG#	Modify List	Date	Phase
1	Shut down for PWM3 pin floating	IF the PWM3 no used, please pull high it for +5VS and not floating	0.1	P.55	(1)Add PR638(0_0603_5%) between PWM3 and +5VS (2)connect the ISNG to +5VS	2010-03-29	DVT
2	OVP problem with PWR and HW side	If the HW side is 0V, through the jumper will cause the sense pin to over the votage setting and it may happen OVP problem.	0.1	P.55	Change the +VGFX_CORE to +VGFX_COREP	2010-03-29	DVT
3							

COMPAL ELECTRONICS

Title

<Title> PIR POWER1

Size A

Document Number PAW00 (LA-6361P)

Rev0.1

Date:

Friday, August 27, 2010

Sheet 55 of 59

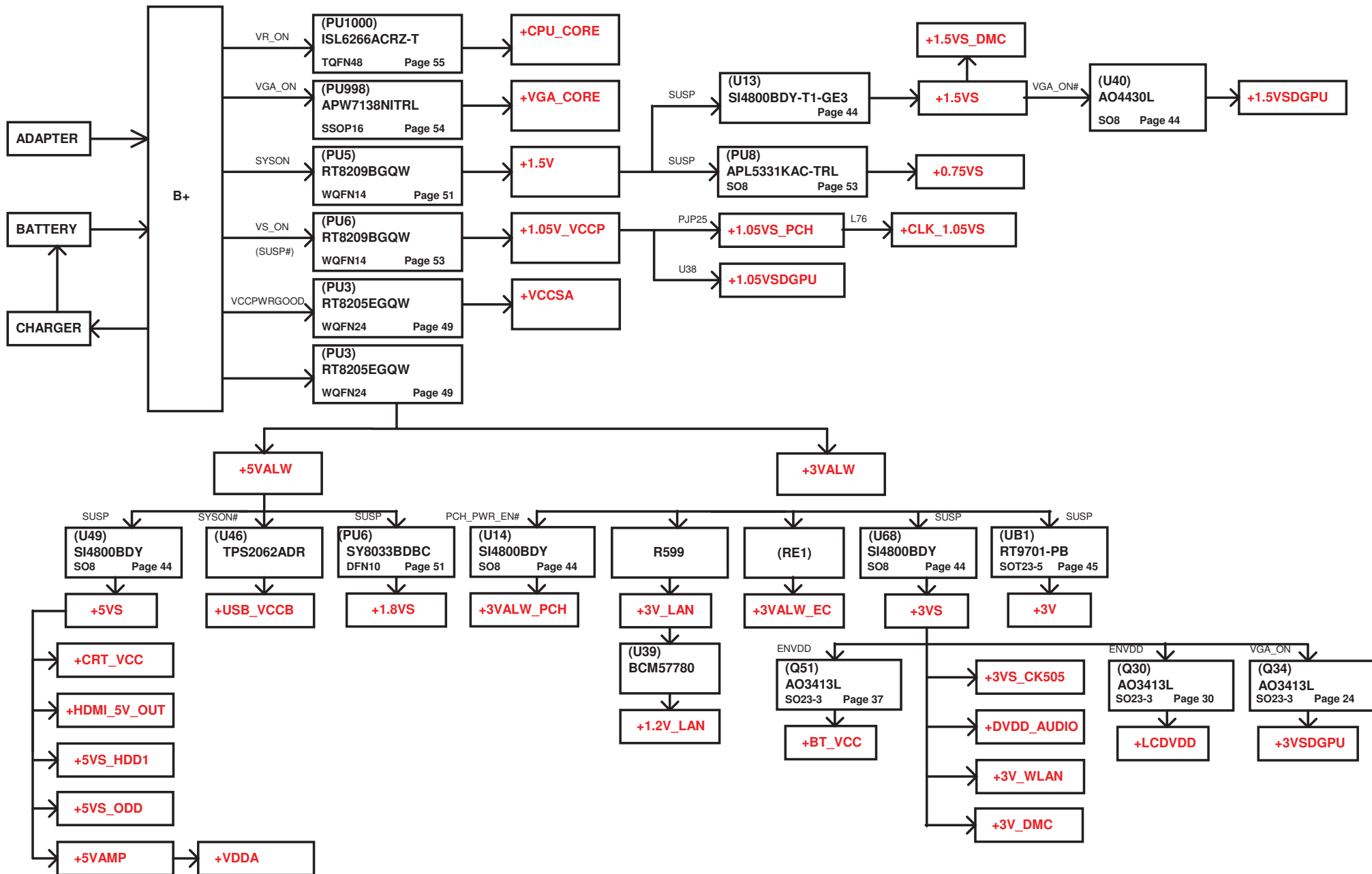
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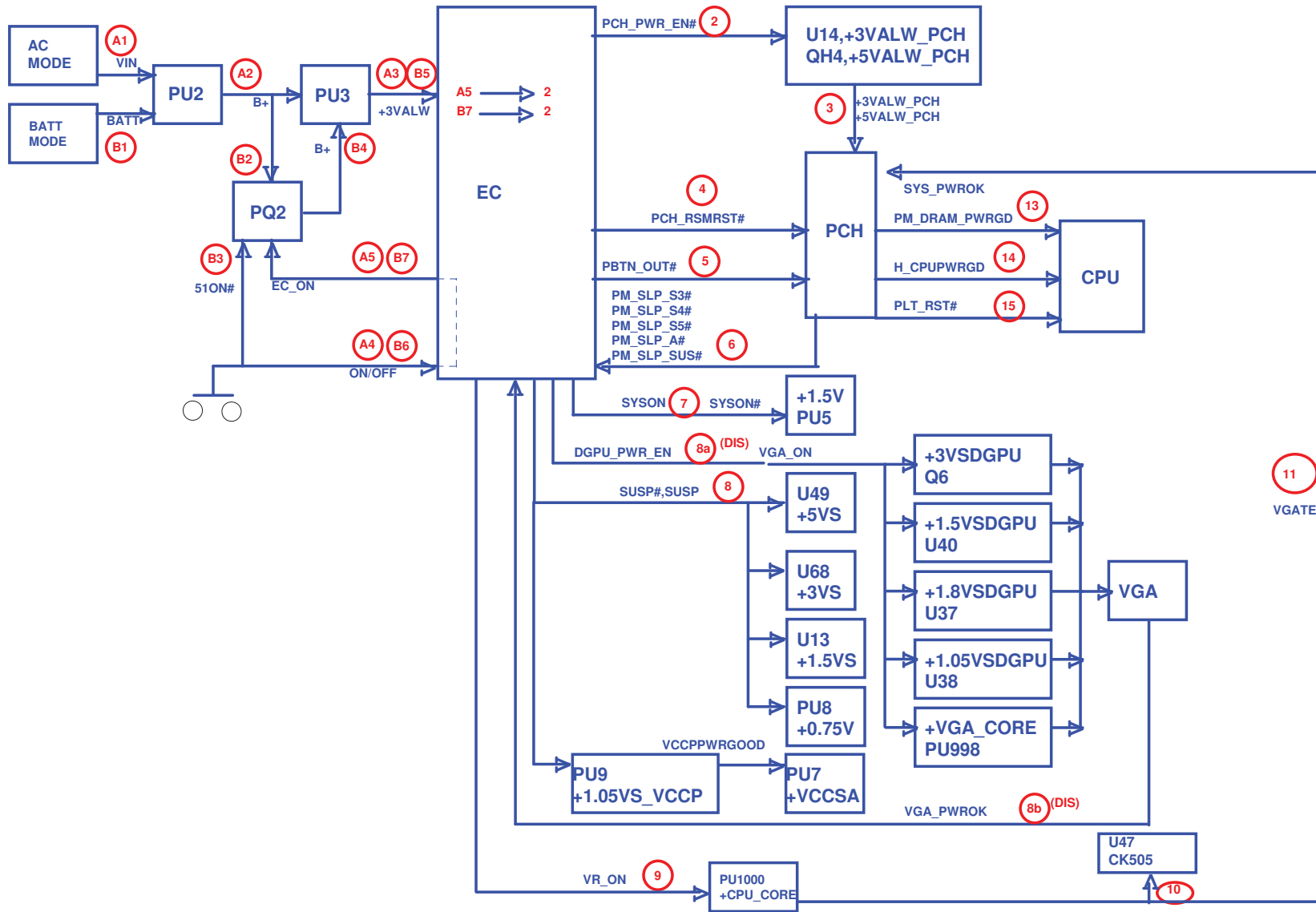
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1





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				Custom	PSWE0 M/B LA-6901P Schematic
				Date	Friday, August 27, 2010
				Sheet	57 of 59
				Rev	0.1

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				Custom	0.1
				Document Number P5WE0 M/B LA-6901P Schematic	
Date:	Friday, August 27, 2010	Sheet	58	of	59

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				Custom	0.1
				Document Number	
				P5WE0 M/B LA-6901P Schematic	
Date:	Friday, August 27, 2010	Sheet	59	of	59